

100Gb/s CFP2 LR4 1310nm 10km Optical Transceiver

Features

- Compliant with 100GBASE-LR4
- Support line rates from 103.125 Gb/s to 111.81 Gb/s
- Integrated LAN WDM TOSA / ROSA for up to 10 km reach over SMF
- CAUI(10x10G) Electrical Interface and 4-lane 25.78Gb/s optical interface
- Duplex LC optical receptacle
- Support Digital Diagnostic Monitoring interface
- No external reference clocked
- RoHS- 10 compliant and lead-free
- Single +3.3V power supply
- Maximum power consumption 6.0W
- All-metal housing for superior EMI performance
- Operating case temperature: 0~70°C

Applications

- Data Center
- Local Area Network (LAN)
- Ethernet switches and router applications

Description

The CFP4-100G-LR4 optical transceiver integrates receiver and transmitter path on one module. In the transmit side, four lanes of serial data streams are recovered, re-timed, and passed to four laser drivers. The laser drivers control four EMLs (Electric-absorption Modulated Lasers) with center wavelength of 1296nm, 1300nm, 1305nm and 1309nm. The optical signals are multiplexed to a single - mode fiber through an industry standard LC connector. In the receive side, the four lanes of optical data streams are optically de-multiplexed by the integrated optical de-multiplexer. Each data stream is recovered by a PIN photo-detector and trans-impedance amplifier, re-timed. This module features a hot-pluggable electrical interface, low power consumption and MDIO management interface.

The module provides an aggregated signaling rate from 103.125Gb/s to 111.81Gb/s. It is compliant with IEEE 802.3ba 100GBASE-LR4 and ITU-T G.959.1, and OIF CEI-28G-VSR. The MDIO management interface complies with IEEE 802.3 Clause 45 standard. The transceiver complies with CFP MSA CFP4 Hardware Specification, CFP MSA Management Interface Specification, and OIF CEI-28G-VSR standards. A block diagram is shown in Figure 1.

Absolute Maximum Ratings

Table1-Absolute Maximum Ratings						
Parameter	Symbols	Min.	Typical	Max.	Unit	Notes
Storage Temperature	TSTG	-40		+85	°C	
Operating Relative Humidity (non-condensing)	RH	5		95	%	
Power Supply Voltage	VCC	-0.5		4.0	V	
Damage Threshold,each Lane	TH _d			5.5	dBm	

Recommended Operating Conditions

Table2-Recommended Operating Conditions						
Parameter	Symbols	Min.	Typical	Max.	Unit	Notes
Operating Case Temperature	Top	0		+70	°C	
Power Supply Voltage	VCC	3.135	3.3	3.465	V	
Data Rate			100		Gb/s	
Control Input Voltage High		2		Vcc	V	
Control Input Voltage Low		0		0.8	V	
Link Distance	D			10	km	

Electrical Characteristics

Table3-Electrical Characteristics						
Parameter	Symbols	Min.	Typical	Max.	Unit	Notes
Low speed control and sense signals, 3.3 V LVCMOS						
Outputs low voltage	VOL			0.2	V	
Output high voltage	VOH	Vcc-0.3		Vcc+0.3	V	
Input low voltage	VIL	-0.3		0.8	V	
Input high voltage	VIH	2		Vcc+ 0.3	V	
Input leakage current	IIN	- 10		10		
Low speed control and sense signals, 1.2 V LVCMOS						
Outputs low voltage	VOL	-0.3		0.2	V	
Output high voltage	VOH	1.0		1.5	V	
Output low current	IOL	4			mA	
Output high current	IOH			-4	mA	
Input low voltage	VIL	-0.3		0.36	V	
Input high voltage	VIH	0.84		1.5	V	
Input leakage current	IIN	- 100		100	μ A	
Input capacitance	C			10	pF	
MDC clock rate		0.1		4	MHz	
High Speed Transmitter electrical input from host						
Differential voltage pk-pk				900	mV	
Common mode noise (rms)				17.5	mV	
Differential termination mismatch				10	%	
Transition time		10			ps	20/80%
Common mode voltage		-0.3		2.8	V	
Eye width	EW15	0.46			UI	At10- 15p robability
Eye height	EH15	100			mV	
High Speed Receiver electrical output to host						
Differential voltage pk-pk				900	mV	
Common mode noise (rms)				17.5	mV	
Differential termination mismatch				10	%	
Transition time		9.5			ps	20/80%
Vertical eye closure	VEC			6.5	dB	

Eye width	EW15	0.57			UI	At10- 15p robability
Eye height	EH15	240			mV	

Optical Characteristic

Table4-Optical Characteristic

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Voltage	Vcc	3.14		3.47	V	
Supply current	Icc			1.8	A	
Power Consumption	Pwr			6.0	W	
Power dissipation (low power mode)	Plp			2.0	W	
Transmitter						
Center Wavelength Range	L1	1294.53	1295.56	1296.59	nm	
	L2	1299.02	1300.05	1301.09	nm	
	L3	1303.54	1304.58	1305.63	nm	
	L4	1308.09	1309.14	1310.09	nm	
Signaling rate, each lane			25.78125		GBd	
Rate tolerance		-100		100	ppm	
Side-mode suppression ratio	SMSR	30				
Total launch power				10.5	dBm	
Average launch power, each lane	Pavg	-4.3		4.5	dBm	
Extinction Ratio	ER	4	9		dB	
Optical modulation amplitude, each lane (OMA)	OMA	-1.3		4.5	dBm	
Difference in launch power between any two lanes (OMA)				5	dB	
Transmitter and Dispersion Penalty, each lane	TDP			2.2	dB	
OMA minus TDP, each lane	OMA-TDP	-2.3			dBm	
Average launch power of OFF transmitter, each lane				-30	dBm	
Transmitter reflectance				-12	dB	
Eye Mask {X1, X2, X3, Y1, Y2, Y3}	{0.25、0.4、0.45、0.25、0.28、0.4}					

Receiver						
Signaling rate, each lane			25.78125		GBd	
Rate tolerance		-100		100	ppm	
Average receive power, each lane channel)	Pavg	-10.6		4.5	dBm	
Receive power, each lane (OMA)				4.5	dBm	
Difference in receiver power between any two lanes (OMA)				5.5	dB	
Receiver Sensitivity (OMA),each lane	Rsen			-8.6	dBm	
Stressed Receiver Sensitivity (OMA), each lane	SRS			-6.8	dBm	1
Vertical eye closure penalty, each lane	VECP		1.8		dB	
Stressed sys J2 jitter, each lane	J2		0.3		UI	2
Stressed sys J9 jitter, each lane	J9		0.47		UI	2
Receiver reflectance				-26	dB	
LOS Assert	Plos_on	-30			dBm	
LOS De-assert	Plos_off			-12		
LOS Hysteresis		0.5		4	dB	

Notes:

[1] Receiver sensitivity (OMA), each lane, is informative.

[2] Vertical eye closure penalty, stressed eye J2 Jitter, and stressed eye J9 Jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Digital Diagnostic Functions

Table5-Digital Diagnostic Functions

Parameter	Symbols	Min.	Max	Units	Notes
Temperature monitor absolute error	DMI_Temp	-3	+3	degC	Over operating temperature range
Supply voltage monitor absolute error	DMI_VCC	-0.15	0.15	V	Over full operating range
Channel RX power monitor absolute error	DMI_RX_Ch	-2	2	dB	1
Channel Bias current monitor	DMI_Ibias_Ch	-10%	10%	mA	
Channel TX power monitor absolute error	DMI_TX_Ch	-2	2	dB	1

Notes:

[1] Due to measurement accuracy of different single mode fibers, there could be an additional +/-1 dB fluctuation, or a +/- 3 dB total accuracy.

17	LVC MOS1	PRG_CNTL1	Programmable control 1; MSA default: TRXIC_RSTn; “0” : reset; “1” or NC: not used
18	LVC MOS1	PRG_CNTL2	Programmable control 2; MSA default: Hardware interlock LSB; Default “0” : $\leq 9\text{ W}$
19	LVC MOS1	PRG_CNTL3	Programmable control 3; MSA default: Hardware interlock MSB; Default “1” : $\leq 9\text{ W}$
20	LVC MOS	PRG_ALARM1	Programmable alarm 1; MSA default: HIPWR_ON; “1” : module power up completed, “0” : module not high powered up
21	LVC MOS	PRG_ALARM2	Programmable alarm 2; MSA default: MOD_READY, “1” : Ready, “0” : not Ready
22	LVC MOS	PRG_ALARM3	Programmable alarm 3; MSA default: MOD_FAULT, “1” : Fault, “0” : no Fault
23		GND	Module ground
24	LVC MOS1	TX_DIS	Transmitter disable for all lanes; “1” or NC: transmitter disabled; “0” : transmitter enabled
25	LVC MOS	RX_LOS	Receiver loss of optical signal; “1” : low optical signal, “0” : normal condition
26	LVC MOS1	MOD_LOPWR	Module low power mode; “1” or NC: module in low power mode, “0” : power on enabled
27	GND	MOD_ABS	Module absent; “1” or NC: module absent; “0” : module present. Pull up resistor on host.
28	LVC MOS2	MOD_RSTn	Module reset; “0” : reset the module; “1” or NC: module enabled
29	LVC MOS	GLB_ALRMn	Global alarm; “0” : alarm in any MDIO alarm register; “1” : no alarm condition. Pull up resistor on host.
30		GND	Module ground
31	1.2V CMOS	MDC	Management interface clock input
32	1.2V CMOS	MDIO	Management interface bi-directional data
33	1.2V CMOS	PRTADR0	MDIO physical port address bit 0
34	1.2V CMOS	PRTADR1	MDIO physical port address bit 1
35	1.2V CMOS	PRTADR2	MDIO physical port address bit 2
36		VND_IO_C	Module vendor IO C; do not connect
37		VND_IO_D	Module vendor IO D; do not connect
38		VND_IO_E	Module vendor IO E; do not connect
39		3.3V_GND	3.3V ground; tied with module ground
40		3.3V_GND	3.3V ground; tied with module ground
41		3.3V	3.3V module supply voltage
42		3.3V	3.3V module supply voltage
43		3.3V	3.3V module supply voltage
44		3.3V	3.3V module supply voltage
45		3.3V_GND	3.3V ground; tied with module ground
46		3.3V_GND	3.3V ground; tied with module ground
47		N.C.	No connect
48		N.C.	No connect

49		GND	Module ground
50	CML	{RX_MCLKn}	No connect
51	CML	{RX_MCLKp}	No connect
52		GND	Module ground
53		GND	Module ground
54		N.C.	No connect
55		N.C.	No connect
56		GND	Module ground
57		RX0P	25 Gbps receiver data; Lane 0
58		RX0n	25 Gbps receiver data bar; Lane 0
59		GND	Module ground
60		RX1p	25 Gbps receiver data; Lane 1
61		RX1n	25 Gbps receiver data bar; Lane 1
62		GND	Module ground
63		N.C.	No connect
64		N.C.	No connect
65		GND	Module ground
66		N.C.	No connect
67		N.C.	No connect
68		GND	Module ground
69		RX2p	25 Gbps receiver data; Lane 2
70		RX2n	25 Gbps receiver data bar; Lane 2
71		GND	Module ground
72		RX3p	25 Gbps receiver data; Lane 3
73		RX3n	25 Gbps receiver data bar; Lane 3
74		GND	Module ground
75		N.C.	No connect
76		N.C.	No connect
77		GND	Module ground
78	CML	{REFCLKp}	Module reference clock. No connect.
79	CML	REFCLKn}	Module reference clock. No connect.
80		GND	Module ground
81		N.C.	No connect
82		N.C.	No connect
83		GND	Module ground
84		TX0p	25 Gbps transmitter data; Lane 0
85		TX0n	25 Gbps transmitter data bar; Lane 0
86		GND	Module ground
87		TX1p	25 Gbps transmitter data; Lane 1

88		TX1n	25 Gbps transmitter data bar; Lane 1
89		GND	Module ground
90		N.C.	No connect
91		N.C.	No connect
92		GND	Module ground
93		N.C.	No connect
94		N.C.	No connect
95		GND	Module ground
96		TX2p	25 Gbps transmitter data; Lane 2
97		TX2n	25 Gbps transmitter data bar; Lane 2
98		GND	Module ground
99		TX3p	25 Gbps transmitter data; Lane 3
100		TX3n	25 Gbps transmitter data bar; Lane 3
101		GND	Module ground
102		N.C.	No connect
103		N.C.	No connect
104		GND	Module ground
1. Pulled up with 4.7 k Ω –10 k Ω to 3.3 V inside the module.			
2. Pulled down with 4.7 k Ω – 10 k Ω to GND inside the module			

Transceiver Block Diagram

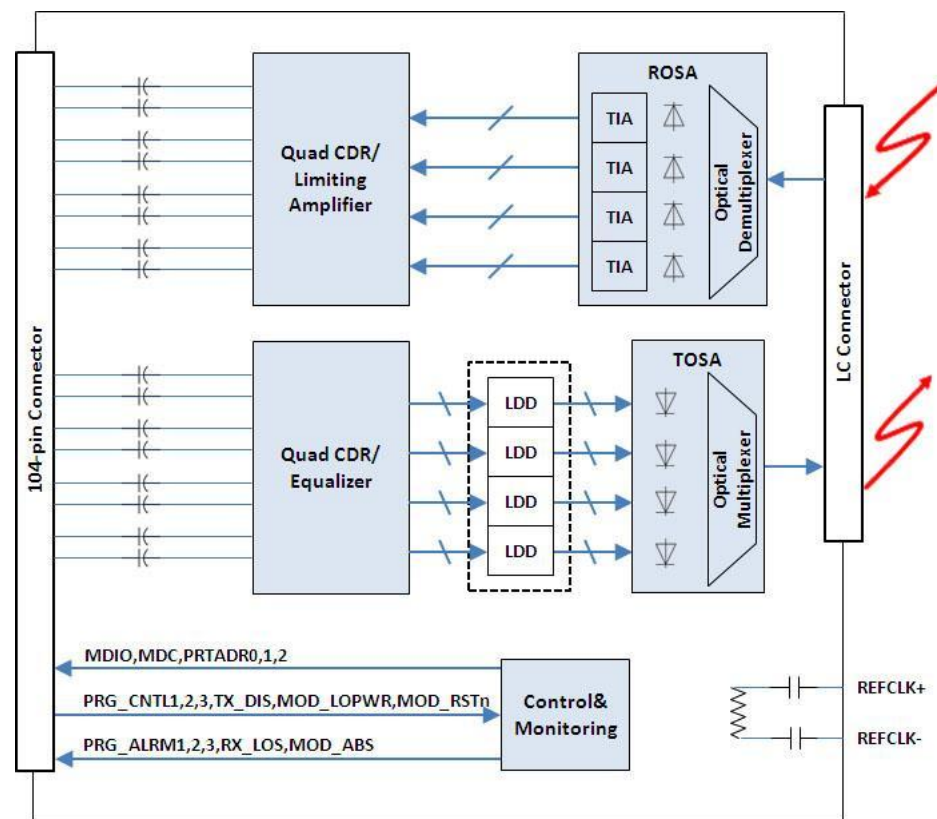


Figure 2 Transceiver Block Diagram

Transmitter

The transmitter path converts four lanes of serial NRZ electrical data from line rate of 25.78 Gbps to 27.95 Gbps to a standard compliant optical signal. Each signal path accepts a 100 Ω differential 100 mV peak-to-peak to 900 mV peak-to-peak 25 Gbps electrical signal on TDxn and TDxp pins. Inside the module, each differential pair of electric signals is input to a CDR (clock-data recovery) chip. The recovered and retimed signals are then passed to a laser driver which transforms the small swing voltage to an output modulation that drives a EML laser. The laser drivers control four EMLs with center wavelengths of 1296 nm, 1300 nm, 1305 nm and 1309 nm. The optical signals from the four lasers are multiplexed together optically. The combined optical signals are coupled to single-mode optical fiber through an industry standard LC optical connector.

Receiver

The receiver takes incoming combined four lanes optical data from line rate of 25.78 Gbps to 27.95 Gbps through an industry standard LC optical connector. The four incoming wavelengths are separated by an optical de-multiplexer into four separated channels. Each output is coupled to a PIN photo-detector. The electrical currents from each PIN photo-detector are converted to a voltage with a high-gain transimpedance amplifier. The electrical output is recovered and retimed by the CDR chip. The four lanes of reshaped electrical signals are output to RDxp and RDxn pins.

Low Speed Signaling

Low speed signaling is based on low voltage CMOS (LVCMOS) operating at a nominal voltage of 3.3 V for the control and alarm signals, and at a nominal voltage of 1.2 V for MDIO address, clock and data signals. All low speed inputs and outputs are based on the CFP MSA CFP2 Hardware Specification Rev. 1.0 and CFP MSA Management Interface Specification Rev. 2.2 requirements. MDC/MDIO: Management interface clock and data lines.

MDC/MDIO: Management interface clock and data lines.

PRTADR0, 1, 2: Input pins. MDIO physical port addresses.

GLB_ALEmn: Output pin. When asserted low indicates that the module has detected an alarm condition in any MDIO alarm register.

PRG_CNTL1, 2, 3: Input pins. Programmable control lines defined in the CFP MSA Management Interface Specification. Pulled up with 4.7 k Ω to 10 k Ω resistors to 3.3 V inside the CFP2 module. TX_Disable: Input pin. When asserted high or left open the transmitter output is turned off. When Tx_Disable is asserted low or grounded the module transmitter is operating normally. Pulled up with 4.7 k Ω to 10 k Ω resistors to 3.3 V inside the CFP2 module.

MOD_LOPWR: Input pin. When asserted high or left open the CFP2 module is in low power mode. When asserted low or grounded the module is operating normally. Pulled up with 4.7 k Ω to 10 k Ω resistors to 3.3 V inside the CFP2 module.

MOD_RSTn: Input pin. When asserted low or grounded the module is in Reset mode. When asserted high or left open the CFP2 module is operating normally after an initialization process. Pulled down with 4.7 k Ω to 10 k Ω resistors to ground inside the CFP2 module.

PRG_ALRM1, 2, 3: Output pins. Programmable alarm lines defined in the CFP MSA Management Interface Specification.

Mod_ABS: Output pin. Asserted high when the CFP2 module is absent and is pulled low when the CFP2 module is inserted.

RX_LOS: Output pin. Asserted high when insufficient optical power for reliable signal reception is received.

Mechanical Dimensions

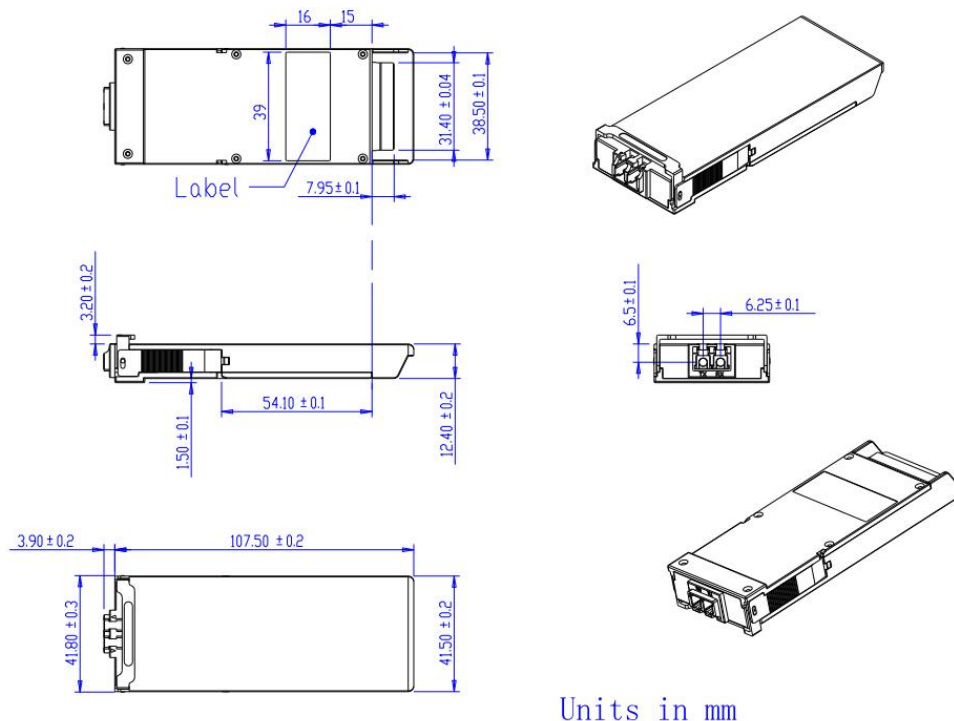


Figure 3 Mechanical Dimensions

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