400Gb/s OSFP XDR4 1310nm 2km MTP/MPO SMF Optical Transceiver

Features

- Supports 425Gbps
- Up to 2km over SMF
- MPO-12 connector
- 8x53.125GBd (PAM4) electrical interface
- OSFP MSA compliant
- PIN and TIA array on the receiver side
- Power dissipation＜12W
- Case temperature range: 0°C to 70°C(commercial)
- Safety Certification: TUV/UL/FDA
- RoHS Compliant

Applications

- 400G Ethernet
- 4 x 100G-DR4+ applications
- Data Center and Enterprise Networking

General Description

The OSFP transceiver module is designed for use in 400 Gigabit Ethernet links over 2km single mode fiber. The module has 8 independent electrical input/output channels at host side with data rate of 53.125Gbps per channel. The integrated GearBox in module converts the 8 channels of 53.125Gbps (PAM4) electrical input data to 4 channels of parallel optical signals, each capable of 106.25Gbps (PAM4) operation for an aggregate data rate of 425Gbp/s. The four transmitter/receiver units operate on 1310nm wavelengths. The electrical interface of the module is compliant with the 400GAUI-8 interface as defined by IEEE 802.3bs, and compliant with OSFP MSA.

Absolute Maximum Ratings

Table1-Absolute Maximum Ratings

Parameter	Symbols	Min.	Typical	Max.	Unit	Notes
Storage Temperature	TS	-40		85	ºC	
Supply Voltage	VCC	-0.5		3.6	V	
Relative Humidity (Non-condensing)	RH	5		95	%	
Data Input Voltage Differential	lVDIP-VDINl			1	V	
Control Input Voltage	VI	-0.3		VCC+0.5	V	
Control Output Current	IO	-20		20	mA	

Recommended Operating Conditions

Table2-Recommended Operating Conditions

Parameter	Symbols	Min.	Typical	Max.	Unit	Notes
Operating Case Temperature	TOPR	0		70	°C	
Power Supply Voltage	VCC	3. 135	3.3	3.465	V	
Instantaneous Peak Current at Hot Plug	ICC_IP			5600	mA	
Sustained Peak Current at Hot Plug	ICC_SP			4620	mA	
Maximum Power Dissipation	PD			14	W	
Maximum Power Dissipation, Low Power Mode	PDLP			1.5	W	
Signaling Speed per Lane	DRL		26.5625		GBd	
Control Input Voltage High	VIH	VCC*0.7		VCC+0.3	V	
Control Input Voltage Low	VIL	-0.3		VCC*0.3	V	
Two Wire Serial Interface Clock Rate				400	kHz	
Power Supply Noise				66	mVpp	
Rx Differential Data Output Load			100		Ohm	
Operating Distance		2		10000	m	

Electrical Characteristic

Table3-Electrical Characteristic

Parameter	Min.	Typical	Max.	Unit	Notes
Transmitter					
Differential Pk-pk Input Voltage Tolerance	900			mv	
Differential Termination Mismatch			10	%	
Single-ended Voltage Tolerance Range	-0.4		3.3	V	
DC Common Mode Voltage	-350		2850	mv	
Receiver					
AC Common-mode Output Voltage (RMS)			17.5	mv	
Differential Output Voltage			900	mv	
Near-end Eye height, Differential	70			mv	
Far-end Eye Height, Differential	30			mV	
Far-end Pre-cursor Ratio			2.5	%	
Differential Termination Mismatch			10	%	
Transition Time (Min. 20%~80%)	9.5			ps	
DC Common Mode Voltage	-350		2850	mV	

Optical Characteristic

Table4-Optical Characteristic

Parameter	Symbols	Min.	Typical	Max.	Unit	Notes
Transmitter						
Wavelength L0	λ C0	1272.55	1273.55	1274.54	nm	
Wavelength L1	λ C1	1276.89	1277.89	1278.89	nm	
Wavelength L2	λ C2	1281.25	1282.26	1283.27	nm	
Wavelength L3	λ C3	1285.65	1286.67	1287.68	nm	
Wavelength L4	λ C4	1294.53	1295.56	1296.59	nm	
Wavelength L5	λ C5	1299.02	1300.06	1301.09	nm	
Wavelength L6	λ C6	1303.54	1304.59	1305.63	nm	
Wavelength L7	λ C7	1308.09	1309. 14	1310. 19	nm	
Side Mode Suppression Ratio	SMSR	30			dB	
Total Average Launch Power	AOPT			13.2	dBm	
Average Launch Power, each lane	AOPL	-2.8		5.3	dBm	1
Outer Optical Modulation Amplitude (OMA_{outer}), each Lane	TOMA	0.2		5.7	dBm	
Difference in Launch Power Between Any Two Lanes (OMA_{outer})	DT_OMA			4	dB	

Launch Power in OMA_{outer} Minus TDECQ, each Lane for ER＞4.5dB	TOMA-TDECQ	- 1.2			dBm	
Launch Power in OMAouterMinus TDECQ, each Lane for ER＜4.5dB	TOMA-TDECQ	- 1. 1			dBm	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each Lane	TDECQ			3.3	dB	
Average Launch Power of OFF Transmitter, each Lane	TOFF			-30	dBm	
Extinction Ratio	ER	3.5			dB	
RIN15. 1 OMA	RIN			- 132	dB/Hz	
Optical Return Loss Tolerance	ORL			15. 1	dB	
Transmitter Reflectance	TR			-26	dB	2
Receiver						
Wavelength L0	λ C0	1272.55	1273.55	1274.54	nm	
Wavelength L1	λ C1	1276.89	1277.89	1278.89	nm	
Wavelength L2	λ C2	1281.25	1282.26	1283.27	nm	
Wavelength L3	λ C3	1285.65	1286.67	1287.68	nm	
Wavelength L4	λ C4	1294.53	1295.56	1296.59	nm	
Wavelength L5	λ C5	1299.02	1300.06	1301.09	nm	
Wavelength L6	λ C6	1303.54	1304.59	1305.63	nm	
Wavelength L7	λ C7	1308.09	1309. 14	1310. 19	nm	
Damage Threshold, each Lane	AOPD	6.3			dBm	
Average Receive Power, each Lane	AOPR	-9. 1		5.3	dBm	
Receive Power (OMA_{outer}), each Lane	OMAR			5.7	dBm	
Difference in Receive Power Between Any Two Lanes (OMA_{outer})	DR_OMA			4.5	dB	
Receiver Reflectance	RR			-26	dB	
Receiver Sensitivity(OMA_{outer}), each Lane	SOMA			-7. 1	dBm	3
Stressed Receiver Sensitivity (OMA_{outer}), each Lane	SRS			-4.7	dBm	4

Notes

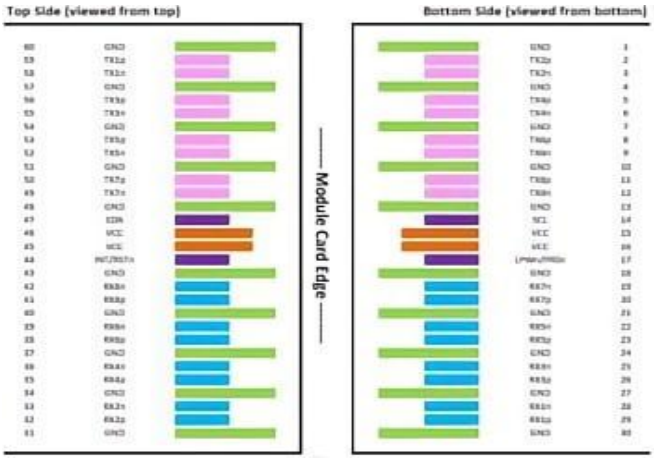
1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength.

2. Transmitter reflectance is defined looking into the transmitter.

3. Receiver sensitivity (OMA_{outer}), each lane (max) is informative and is defined for a transmitter with SECQ of 0.9 dB.

4. Measured with conformance test signal at TP3 for the BER = $2.4x\ 10^{-4}$

Pin Description



Pin Function Definitions

Table5- Pin Function Definitions

Pin	Symbol	Description	Logic	Notes
1	GND	Ground		
2	TX2p	Transmitter Data Non-Inverted	CML-I	
3	TX2n	Transmitter Data Inverted	CML-I	
4	GND	Ground		
5	TX4p	Transmitter Data Non-Inverted	CML-I	
6	TX4n	Transmitter Data Inverted	CML-I	
7	GND	Ground		
8	TX6p	Transmitter Data Non-Inverted	CML-I	
9	TX6n	Transmitter Data Inverted	CML-I	
10	GND	Ground		
1 1	TX8p	Transmitter Data Non-Inverted	CML-I	
12	TX8n	Transmitter Data Inverted	CML-I	
13	GND	Ground		
14	SCL	2-wire Serial interface clock	LVCMOS-I/O	
15	VCC	+3.3V Power		
16	VCC	+3.3V Power		
17	LPWn/P RSn	Low-Power Mode / Module Present	Multi-Level	
18	GND	Ground		
19	RX7n	Receiver Data Inverted	CML-O	
20	RX7p	Receiver Data Non-Inverted	CML-O	
21	GND	Ground		
22	RX5n	Receiver Data Inverted	CML-O	
23	RX5p	Receiver Data Non-Inverted	CML-O	

24	GND	Ground		
25	RX3n	Receiver Data Inverted	CML-O	
26	RX3p	Receiver Data Non-Inverted	CML-O	
27	GND	Ground		
28	RX1n	Receiver Data Inverted	CML-O	
29	RX1p	Receiver Data Non-Inverted	CML-O	
30	GND	Ground		
31	GND	Ground		
32	RX2p	Receiver Data Non-Inverted	CML-O	
33	RX2n	Receiver Data Inverted	CML-O	
34	GND	Ground		
35	RX4p	Receiver Data Non-Inverted	CML-O	
36	RX4n	Receiver Data Inverted	CML-O	
37	GND	Ground		
38	RX6p	Receiver Data Non-Inverted	CML-O	
39	RX6n	Receiver Data Inverted	CML-O	
40	GND	Ground		
41	RX8p	Receiver Data Non-Inverted	CML-O	
42	RX8n	Receiver Data Inverted	CML-O	
43	GND	Ground		
44	INT/RSTn	Module Interrupt / Module Reset	Multi- Level	
45	VCC	+3.3V Power		
46	VCC	+3.3V Power		
47	SDA	2-wire Serial interface data	LVCM OS-I/O	
48	GND	Ground		
49	TX7n	Transmitter Data Inverted	CML-I	
50	TX7p	Transmitter Data Non-Inverted	CML-I	
51	GND	Ground		
52	TX5n	Transmitter Data Inverted	CML-I	
53	TX5p	Transmitter Data Non-Inverted	CML-I	
54	GND	Ground		
55	TX3n	Transmitter Data Inverted	CML-I	
56	TX3p	Transmitter Data Non-Inverted	CML-I	
57	GND	Ground		
58	TX1n	Transmitter Data Inverted	CML-I	
59	TX1p	Transmitter Data Non-Inverted	CML-I	
60	GND	Ground		

Timing for Soft Control and Status Functions

Parameter	Symbols	Min.	Max.	Unit	Notes
MgmtInit Duration			2000	ms	
ResetL Assert Time	t_reset_init	10		μs	
IntL Assert Time	ton_IntL		200	ms	
IntL De-assert Time	toff_IntL		500	μs	
Rx LOS Assert Time (Fast Mode)	ton_losf		N/A	ms	Not Supported
Rx LOS De-assert (Fast Mode)	toff_losf		N/A	ms	Not Supported
Tx Fault Assert Time	ton_Txfault		200	ms	
Flag Assert Time	ton_flag		200	ms	
Mask Assert Time	ton_mask		100	ms	
Mask De-assert Time	toff_mask		100	ms	
Module Select Wait Time	ModSelL WaitTime		N/A		Not Supported

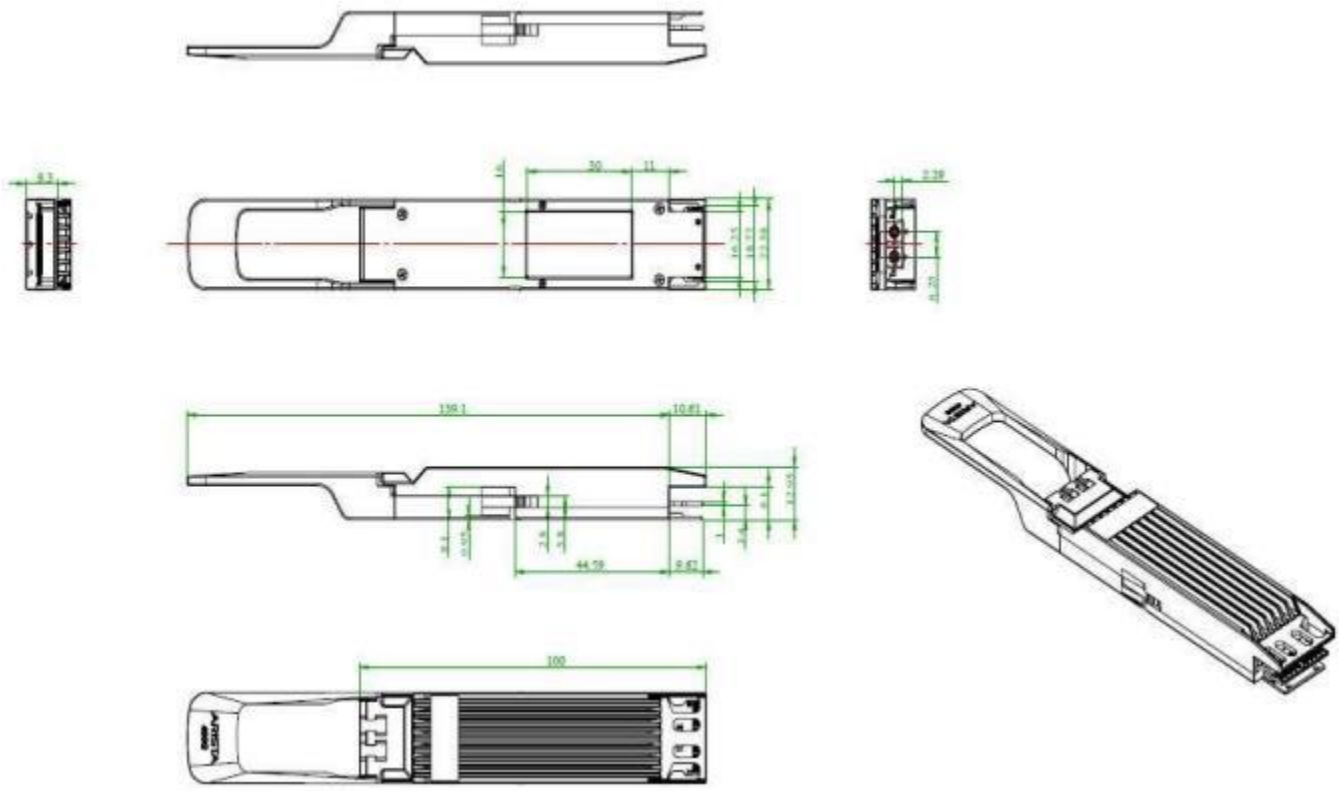
I/O Timing for Squelch and Disable

Parameter	Symbols	Max.	Unit	Notes
Rx Squelch Assert Time	ton_Rxsq	15	ms	
Rx Squelch De-assert Time	toff_Rxsq	1500	ms	
Tx Squelch Assert Time	ton_Txsq	400	ms	
Tx Squelch De-assert Time	toff_Txsq	1000	ms	Based on Modulation
Tx Disable Assert Time (Fast Mode)	ton_Txdisf	N/A	ms	Not Supported
Tx Disable De-assert Time(Fast Mode)	toff_Txdisf	N/A	ms	Not Supported
Rx Output Disable Assert Time	ton_Rxdis	100	ms	
Rx Output Disable De-assert Time	toff_Rxdis	100	ms	
Squelch Disable Assert Time	ton_sqdis	N/A	ms	Not Supported
Squelch Disable De-assert Time	toff_sqdis	N/A	ms	Not Supported

Digital Diagnostics

Parameter	Range	Accuracy.	Unit	Calibration
Temperature	0~70	±3	°C	Internal
Voltage	0~VCC	0. 1	V	Internal
Tx Bias Current (each Lane)	0~ 100	10%	mA	Internal
Tx Output Power (each Lane)	-2.8~5.3	±3	dB	Internal
Rx Receive Power (each Lane)	-9. 1~5.3	±3	dB	Internal

Mechanical Dimensions



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