40G QSFP+ to 8x LC Connector Breakout Active Optical Cable

Features

- Transmission data rate up to 10.3Gbit/s per channel
- Connector 1: QSFP+
- Connector 2: LC/SC/ST/FC Connector(8)
- Full duplex 4 channel 850nm parallel active optical cable
- Available lengths (in meters): 1, 2, 3, 4, 5....
- SFF-8436 QSFP+ compliant housing and hot pluggable electrical int
- Differential AC-coupled high speed data interface
- Management Interface and digital diagnostic monitoring（DDM) through I2C
- Commercial temperature range(COM): 0 to 70°C
- Support Rx output pre-emphasis
- Housing isolated from connector ground
- Low power consumption
- 3.3V power supply voltage
- RoHS 6 compliant

Applications

- 40GBASE-SR4 40G Ethernet
- 4G/ 8G/ 10G Fibre Channel
- Proprietary high speed, high density data transmission
- Creating a breakout cable with four Duplex LC/SC/ST/FC
- connectors for port expander applications
- High performance computing, server and data storage.

Description:

QSFP+ to 8 x LC/SC/ST/FC Connector Breakout Active Optical Cable(AOC) are a high performance, low power consumption, long reach interconnect solution supporting 40G Ethernet, fiber channel and PCIe. It is compliant with the QSFP MSA and IEEE P802.3ba

40GBASE-SR4. QSFP+ Breakout Cable is an assembly of 4 full-duplex lanes, where each lane is capable of transmitting data at rates up to 10Gb/s, providing an aggregated rate of 40Gb/s.

QSFP+ Breakout Cable are suitable for short distances and offer a highly cost-effective way to connect within racks and across adjacent racks. This product is a high data rate parallel active optical cable, to overcome the bandwidth limitation of traditional copper cable.

Absolute Maximum Ratings

Table1-Absolute Maximum Ratings

Parameter	Symbol	Min.	Typical	Max.	Unit	Note
3.3V Supply Voltage	Vcc	3.135	-	3.465	V	
Input Voltage	Vin	-0.3		Vcc+0.3	V	
Operating Case Temperature	Tc	0	-	70	ºC	
Humidity(non-condensing)	Rh	5		95	%	
Data Rate Per Lane	fd	2.5		10.3	Gbps	
Power Dissipation	Pm			1.5	W	

Specifications

Table2-Specifications

Parameter	Symbol	Min.	Typical	Max.	Unit	Note
Differential input impedance	Zin	90	100	110	ohm	
Differential Output impedance	Zout	90	100	110	ohm	
Differential input voltage amplitude a Amplitude	ΔVin	300		1100	mVp-p	
Differential output voltage amplitude	ΔVout	500		800	mVp-p	
Skew	Sw			300	ps	
Bit Error Rate	BR			E- 12		
Input Logic Level High	VIH	2		VCC	V	
Input Logic Level Low	VIL	0		0.8	V	
Output Logic Level High	VOH	VCC-0.5		VCC	V	
Output Logic Level Low	VOL	0		0.4	V	

Notes:

BER=10^-12; PRBS 2^31-1@10.3125Gbps.

Differential input voltage amplitude is measured between TxNp and TxNn.

Differential output voltage amplitude is measured between RxNp and RxNn.

Optical Characteristics

Table3-Optical Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit.	Note
Transmitter						
Center Wavelength	λt	840	850	860	nm	
RMS spectral width	Δλt	-7.5		0.65	nm	
Average launch power, each lane	Pout			2.5	dBm	
				4	dB	
Extinction Ratio	ER	3			dB	
Peak power, each lane				4	dBm	
Transmigrate and dispersion penalty (TDP), each lane	TDP			3.5	dB	
Average launch power of OFF transmitter, each lane				-30	dB	
Eye Mask coordinates:X1, X2, X3, Y1, Y2, Y3	SPECIFICATION VALUES 0.23, 0.34, 0.43, 0.27, 0.35, 0.4				Hit Ratio =5x10-5	
Receiver						
Center Wavelength	λr	840	850	860	nm	
Stressed receiver sensitivity in OMA, each lane				-5.4	dBm	1
Maximum Average power at receiver input, each lane				2.4	dBm	
Receiver Reflectance				- 12	dB	
Peak power, each lane				4	dBm	
LOS Assert		-30			dBm	
LOS De-Assert – OMA				-7.5	dBm	
LOS Hysteresis		0.5			dB	

Note:

1. Measured with conformance test signal at TP3 for BER = 10e-12

Pin Description

Pin	Logic	Symbols	Description	Notes
1		GND	Module Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	
4		GND	Module Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data output	
7		GND	Module Ground	1
8	LVTLL-I	ModSelL	Module Select	
9	LVTLL-I	ResetL	Module Reset	
10		VccRx	+ 3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	
13		GND	Module Ground	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Module Ground	1
17	CML-O	Rx 1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx 1n	Receiver Inverted Data Output	
19		GND	Module Ground	1
20		GND	Module Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Module Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	1
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Module Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3 V Power Supply transmitter	2
30		Vcc1	+3.3 V Power Supply	2
31	LVTTL-I	LPMode	Low Power Mode	
32		GND	Module Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	

34	CML-I	Tx3n	Transmitter Inverted Data Output	
35		GND	Module Ground	1
36	CML-I	Tx 1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx 1n	Transmitter Inverted Data Output	
38		GND	Module Ground	1

Notes:

1. Module circuit ground is isolated from module chassis ground within the module.

2. Open collector; should be pulled up with 4.7k -10k ohms on host board to a voltage between 3. 15Vand 3.6V.

Low Speed Electrical Hardware Pins

In addition to 2-wire serial interface, 40G QSFP+ AOC module has the following low speed pins for control and status:

(1) ModSelL Pin

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial Communication commands. The ModSelL allows the use of multiple QSFP modules on a single 2-wire interface bus. When the ModSelL is "High", the module will not respond to any 2-wire interface communication from the host. ModSelL has an internal pull-up in the module.

(2) ResetL Pin

Reset. LPMode_ Reset has an internal pull- up in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data_ Not_ Ready bit negated. Note that on power up (including hot insertion) the module will post this completion of reset interrupt without requiring a reset.

(3) LP Mode Pin

F-tone QSFP AOC operate in the low power mode (less than 1.5 W power consumption) This pin active high will decrease power consumption to less than 1W.

(4) ModPrsL Pin

ModPrsL is pulled up to Vcc on the host board and grounded in the module. The ModPrsL is asserted "Low"when the module is inserted and deasserted "High" when the module is physically absent from the host connector.

(5) IntL Pin

IntL is an output pin. When "Low", it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt by using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled up to Vcc on the host board.

Power Supply Filtering

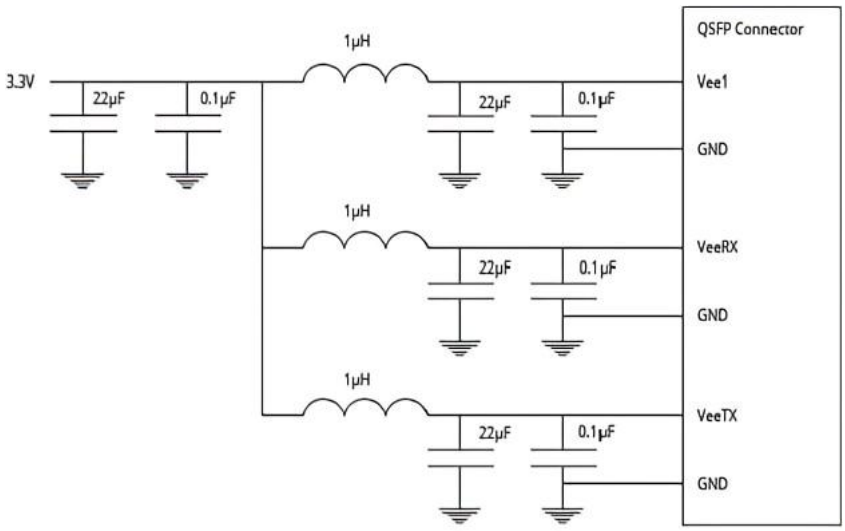
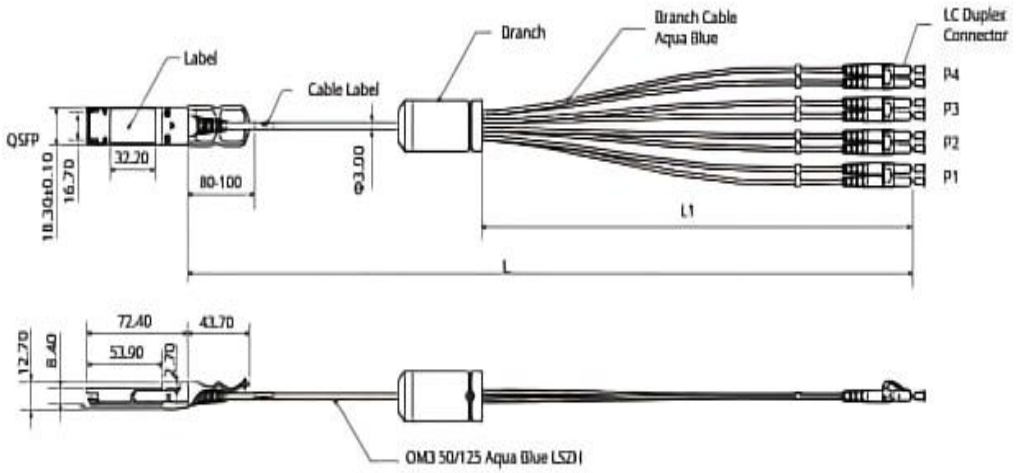


Figure 1. Host Board Power Supply Filtering

Mechanica



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2. Nothing herein should be construed as constituting an additional warranty.

3. NADDOD assumes no responsibility for the use or reliability of equipment or software not provided by NADDOD.