

# 400Gb/s QSFP-DD ER8 1310nm 40Km SMF Optical Transceiver

## Features

- Compliant with IEEE std 802.3cnTM-2019:
  - 400GBASE-ER8 optical interface
  - 400GAUI-8 electrical interface
- Compliant with QSFP-DD MSA HW Rev 5.0 with duplex LC connector
- Compliant with QSFP-DD CMIS Rev 4.0
- Case operating temperature 0°C to 70°C
- Two wire serial Interface with digital diagnostic monitoring
- Complies with EU Directive 2011/65/EU (RoHS compliant)
- Class 1/1M Laser

## Applications

- 400G Ethernet
- Data center Enterprise networking

## Absolute Maximum Ratings

Parameter	Symbols	Min.	Typical	Max.	Unit	Notes
Storage Temperature	TSTG	-40		+85	°C	
Operating Relative Humidity (non-condensing)	RH	5		95	%	
Supply Voltage	VCC	-0.5		3.6	V	
Data Input Voltage Differential	IVDIP-VDINI			1	V	
Control Input Voltage	VI	-0.3		VCC+0.5	V	
Control Output Current	IO	-20		20	mA	

## Recommended Operating Conditions

Parameter	Symbols	Min.	Typical	Max.	Unit	Notes
Case temperature	Tcase	0		+70	°C	
Supply Voltage	VCC	3.135	3.3	3.465	V	
Instantaneous peak current at hot plug	ICC_IP			56000	mA	PAM4
Sustained peak current at hot plug	ICC_SP			4620	mA	
Maximum Power Dissipation	PD			14	W	
Maximum Power Dissipation, Low Power Mode	PDLP			1.5	W	1
Signaling Speed per Lane	DRL		26.5625		GBd	2
Control Input Voltage High	VIH	VCC*0.7		VCC+0.3	V	
Control Input Voltage Low	VIL	-0.30		VCC*0.3	V	
Two Wire Serial Interface Clock Rate				400	kHz	
Power Supply Noise				66	mVpp	
Rx Differential Data Output Load			100		Ohm	
Operating Distance		0.002		40	km	1

Notes:

[1] Channel insertion loss is 18dB for 40km.

## Transmitter Optical Specifications

Table3-Transmitter Optical Specifications						
Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Wavelength L0	$\lambda$ C0	1272.55	1273.55	1274.54	nm	
Wavelength L1	$\lambda$ C1	1276.89	1277.89	1278.89	nm	
Wavelength L2	$\lambda$ C2	1281.25	1282.26	1283.27	nm	
Wavelength L3	$\lambda$ C3	1285.65	1286.67	1287.68	nm	
Wavelength L4	$\lambda$ C4	1294.53	1295.56	1296.59	nm	
Wavelength L5	$\lambda$ C5	1299.02	1300.06	1301.09	nm	
Wavelength L6	$\lambda$ C6	1303.54	1304.59	1305.63	nm	
Wavelength L7	$\lambda$ C7	1308.09	1309.14	1310.19	nm	
Side Mode Suppression Ratio	SMSR	30	-	-	dB	
Total Average Launch Power	AOPT	-	-	14.6	dBm	
Average Launch Power, each lane	AOPL	-0.6	-	5.6	dBm	1
Outer Optical Modulation Amplitude ( $OMA_{outer}$ ), each Lane	TOMA	2.4	-	6.4	dBm	
Difference in Launch Power between any two Lanes ( $OMA_{outer}$ )	DT_OMA	-	-	4	dB	
Launch Power in $OMA_{outer}$ minus TDECQ, each lane	TOMA-TDECQ	1	-	-	dBm	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each lane	TDECQ	-	-	3.4	dB	
TDECQ $-10\log_{10}(C_{eq})$	-	-	-	3.4	dB	
Average Launch Power of OFF Transmitter, each lane	TOFF	-	-	-30	dBm	
Extinction Ratio	ER	6	-	-	dB	
RIN15OMA	RIN	-	-	-132	dB/Hz	
Optical Return Loss Tolerance	ORL	-	-	15	dB	
Transmitter Reflectance	TR	-	-	-26	dB	2

Notes:

[1] Receiver sensitivity ( $OMA_{outer}$ ), each lane (max) is informative and is defined for a transmitter with SECQ of 1.4 dB.

[2] Measured with conformance test signal at TP3 for the BER =  $2.4 \times 10^{-4}$

## Receiver Optical Specifications

**Table4-Receiver Optical Specifications**

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Wavelength L0	$\lambda$ C0	1272.55	1273.55	1274.54	nm	
Wavelength L1	$\lambda$ C1	1276.89	1277.89	1278.89	nm	
Wavelength L2	$\lambda$ C2	1281.25	1282.26	1283.27	nm	
Wavelength L3	$\lambda$ C3	1285.65	1286.67	1287.68	nm	
Wavelength L4	$\lambda$ C4	1294.53	1295.56	1296.59	nm	
Wavelength L5	$\lambda$ C5	1299.02	1300.06	1301.09	nm	
Wavelength L6	$\lambda$ C6	1303.54	1304.59	1305.63	nm	
Wavelength L7	$\lambda$ C7	1308.09	1309.14	1310.19	nm	
Damage Threshold, each Lane	AOPD	-3.4	-	-	dBm	
Average Receive Power, each Lane	AOPR	-18.6	-	-4.4	dBm	
Receive Power ( $OMA_{outer}$ ), each Lane	OMAR	-	-	-3.6	dBm	
Difference in Receive Power between any two Lanes ( $OMA_{outer}$ )	DR_OMA	-	-	5.8	dB	
Receiver Reflectance	TP4	-350		2850	mV	3
Receiver Sensitivity ( $OMA_{outer}$ ), each Lane	RR	-	-	-26	dB	
Stressed Receiver Sensitivity ( $OMA_{outer}$ ), each Lane	SOMA	-	-	Max( - 16.1, SECQ - 17.5)	dBm	1
Conditions of stressed receiver sensitivity test:	SRS	-	-	-14.1	dBm	2
Stressed eye closure for PAM4 (SECQ), lane under test	-	-	3.4	-	dB	
SECQ - $10\log_{10}(Ceq)$ , lane under test	-	-	-	3.4	dB	
$OMA_{outer}$ of each aggressor lane	-	-	-8.3	-	dBm	

**Notes:**

[1] Receiver sensitivity ( $OMA_{outer}$ ), each lane (max) is informative and is defined for a transmitter with SECQ of 1.4 dB.

[2] Measured with conformance test signal at TP3 for the BER =  $2.4 \times 10^{-4}$

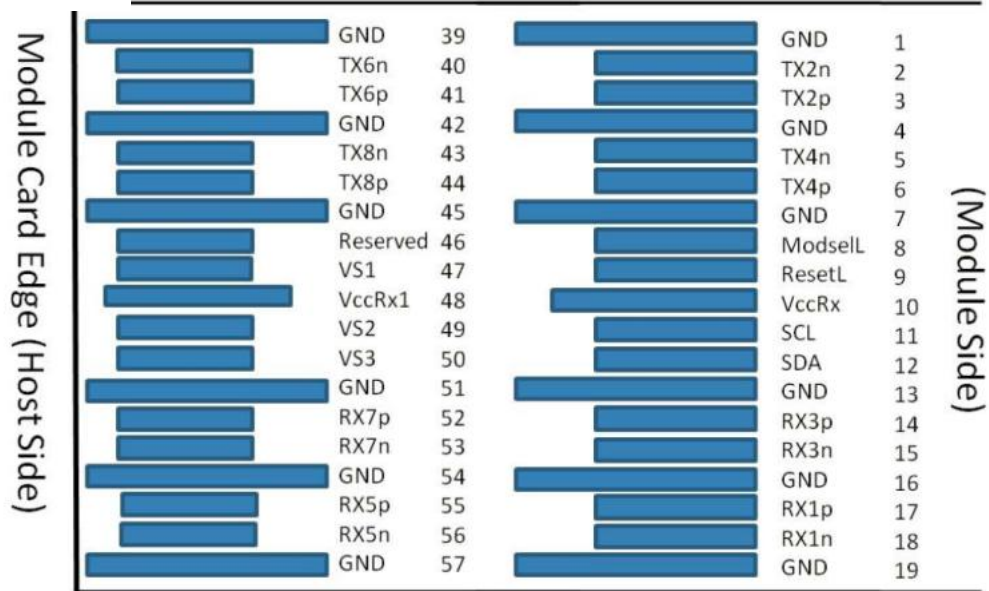
## Electrical Specification High Speed Signal

Table5-Electrical Specification High Speed Signal						
Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
<b>Receiver (Module Output)</b>						
AC common-mode output Voltage(RMS)		-	-	17.5	mV	
Differential output Voltage		-	-	900	mV	
Near-end Eye height, differential		70	-	-	mV	
Far-end Eye height, differential		30	-	-	mV	
Far end pre-cursor ratio		-	-	2.5	%	
Differential Termination Mismatch		-	-	10	%	
Transition Time (min, 20% to 80%)		9.5	-	-	ps	
DC common mode Voltage		-350	-	2850	mV	
<b>Transmitter (Module Input)</b>						
Differential pk-pk input Voltage tolerance		900	-	-	mV	
Differential termination mismatch		-	-	10	%	
Single-ended voltage tolerance range		-0.4	-	3.3	V	
DC common mode Voltage		-350	-	2850	mV	

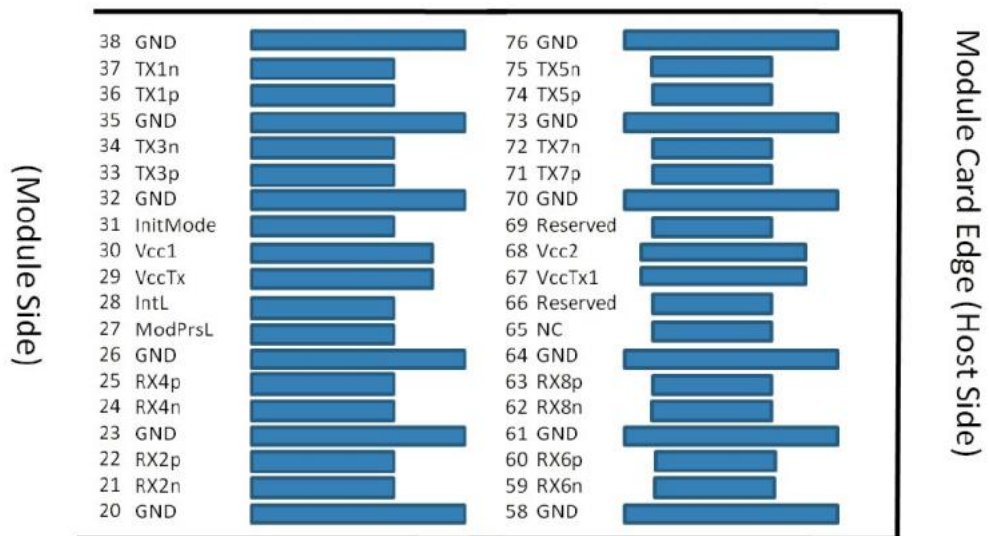
## Electrical Specification Low Speed Signal

Table6-Electrical Specification Low Speed Signal					
Parameter	Symbol	Min.	Max.	Unit	Notes
Module output SCL and SDA	VOL	0	0.4	V	
Module Input SCL and SDA	VIL	-0.3	VCC*0.3	V	
	VIH	VCC*0.7	VCC+0.5	V	
InitMode, ResetL and ModSelL	VIL	-0.3	0.8	V	
	VIH	2	VCC+0.3	V	
IntL	VOL	0	0.4	V	
	VOH	VCC-0.5	VCC+0.3	V	

## Pin Description



Bottom side viewed from bottom



Top side viewed from top

Figure 1 Pin view

## Pin Function Definitions

Table7-Pin Function Definitions

Pin	Logic	Symbol	Description	Notes
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1		GND	Ground	1B
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B
4		GND	Ground	1B
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B
7		GND	Ground	1B
8	LVTTL-I	ModSelL	Module Select	3B
9	LVTTL-I	ResetL	Module Reset	3B
10		Vcc Rx	+3.3V Power Supply Receiver	2B
11	LVC MOS-I/O	SCL	2-wire serial interface clock	3B
12	LVC MOS-I/O	SDA	2-wire serial interface data	3B
13		GND	Ground	1B
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B
15	CML-O	Rx3n	Receiver Inverted Data Output	3B
16		GND	Ground	1B
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B
18	CML-O	Rx1n	Receiver Inverted Data Output	3B
19		GND	Ground	1B
20		GND	Ground	1B
21	CML-O	Rx2n	Receiver Inverted Data Output	3B
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B
23		GND	Ground	1B
24	CML-O	Rx4n	Receiver Inverted Data Output	3B
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B
26		GND	Ground	1B
27	LVTTL-O	ModPrsL	Module Present	3B
28	LVTTL-O	IntL/RxLOSL	Interrupt. Optionally configurable as RxLOSL via the management interface (SFF-8636)	3B
29		VccTx	+3.3V Power supply transmitter	2B
30		Vcc1	+3.3V Power supply	2B
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B
32		GND	Ground	1B
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B
35		GND	Ground	1B
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B
38		GND	Ground	1B
39		GND	Ground	1A
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A

41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A
42		GND	Ground	1A
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A
45		GND	Ground	1A
46		Reserved	For future use	3A
47		VS1	Module Vendor Specific 1	3A
48		VccRx1	3.3V Power Supply	2A
49		VS2	Module Vendor Specific 2	3A
50		VS3	Module Vendor Specific 3	3A
51		GND	Ground	1A
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A
53	CML-O	Rx7n	Receiver Inverted Data Output	3A
54		GND	Ground	1A
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A
56	CML-O	Rx5n	Receiver Inverted Data Output	3A
57		GND	Ground	1A
58		GND	Ground	1A
59	CML-O	Rx6n	Receiver Inverted Data Output	3A
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A
61		GND	Ground	1A
62	CML-O	Rx8n	Receiver Inverted Data Output	3A
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A
64		GND	Ground	1A
65		NC	No Connect	3A
66		Reserved	For future Use	3A
67		VccTx1	3.3V Power Supply	2A
68		Vcc2	3.3V Power Supply	2A
69		Reserved	For future Use	3A
70		GND	Ground	1A
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A
73		GND	Ground	1A
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A
76		GND	Ground	1A



## Recommended QSFP-DD Host Board Schematic

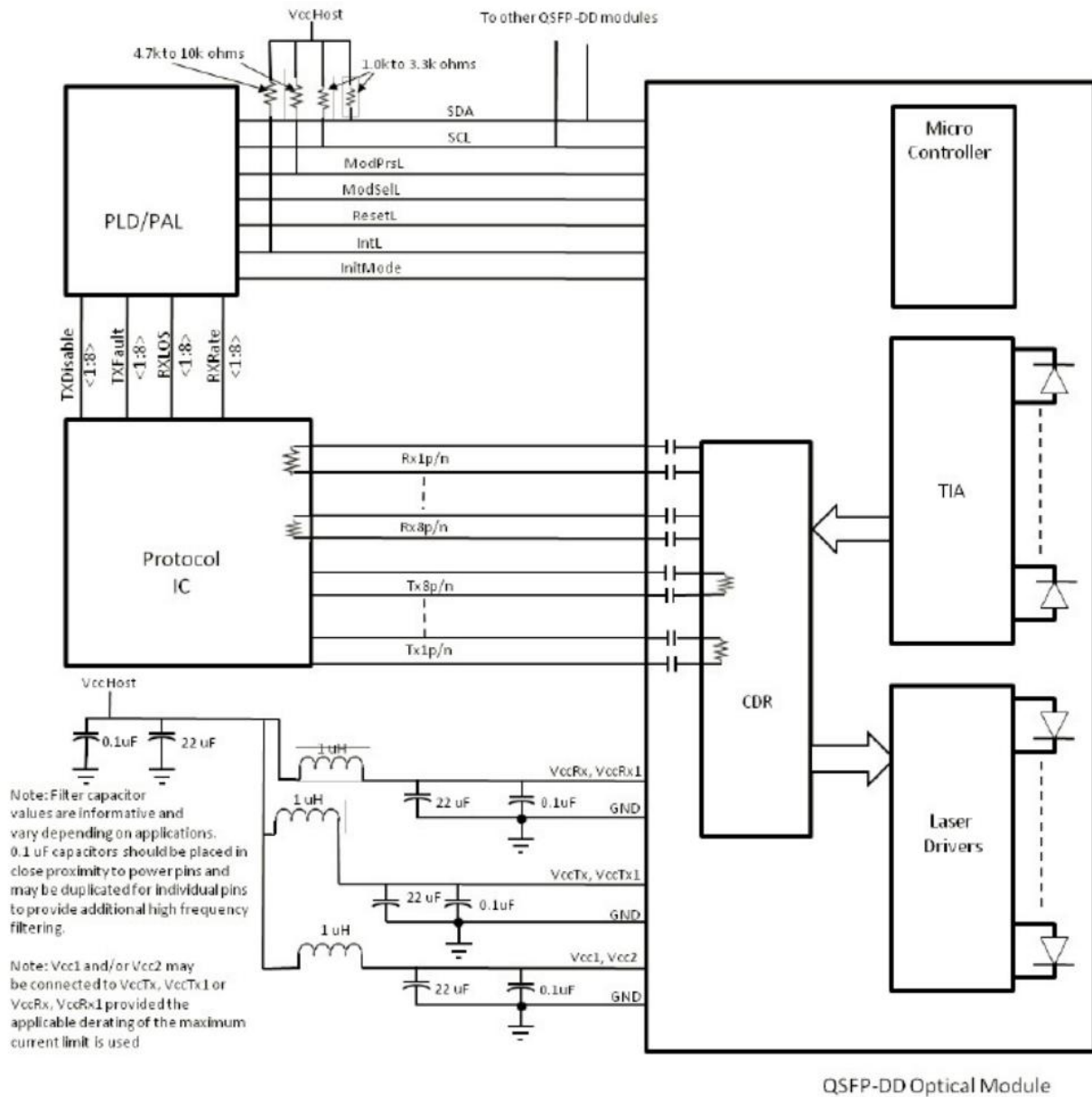


Figure 2 Recommended QSFP-DD Host Board Schematic

## Timing for Soft Control and Status Functions

Table8-Electrical Specification High Speed Signal

Parameter	Symbol	Min.	Max.	Unit	Notes
MgmtInit Duration		-	2000	ms	

ResetL Assert Time	t_reset_init	10	-	μs	
IntL Assert Time	ton_IntL	-	200	ms	
IntL Deassert Time	toff_IntL	-	500	μs	
Rx LOS Assert Time	ton_losf	-	100	ms	
Flag Assert Time	ton_flag	-	200	ms	
Mask Assert Time	ton_mask	-	100	ms	
Mask Deassert Time	toff_mask	-	100	ms	
Module Select Wait Time	ModSelL Wait Time	-	N/A		Not support

## I/O Timing for Squelch and Disable

Table9-I/O Timing for Squelch and Disable

Parameter	Symbol	Min.	Max.	Unit	Notes
Rx Squelch Assert Time	ton_Rxsq	-	50	ms	
Tx Squelch Assert Time	ton_Txsq	-	400	ms	
Tx Squelch Deassert Time	toff_Txsq	-	1500	ms	Based on modulation
Tx Disable Assert Time (fast mode)	ton_Txdisf	-	3	ms	
Tx Disable Deassert Time (fast mode)	toff_Txdisf	-	10	ms	
Rx Output Disable Assert Time	ton_Rxdis	-	100	ms	
Rx Output Disable Deassert Time	toff_Rxdis	-	100	ms	
Squelch Disable Assert Time	ton_sqdis	-	N/A	ms	Not support
Squelch Disable Deassert Time	toff_sqdis	-	N/A	ms	Not support

## Digital Diagnostics

Table10-Digital Diagnostics

Parameter	Range	Accuracy	Units	Notes
Temperature	0 to 70	±3	°C	Internal
Voltage	0 to VCC	0.1	V	Internal
Tx Bias Current (Each Lane)	0 to 100	10%	mA	Internal
Tx Output Power (Each Lane)	-0.6 to +5.6	±3	dB	Internal
Rx Receive Power (Each Lane)	-18.6 to -4.4	±3	dB	Internal

## Mechanical Dimensions

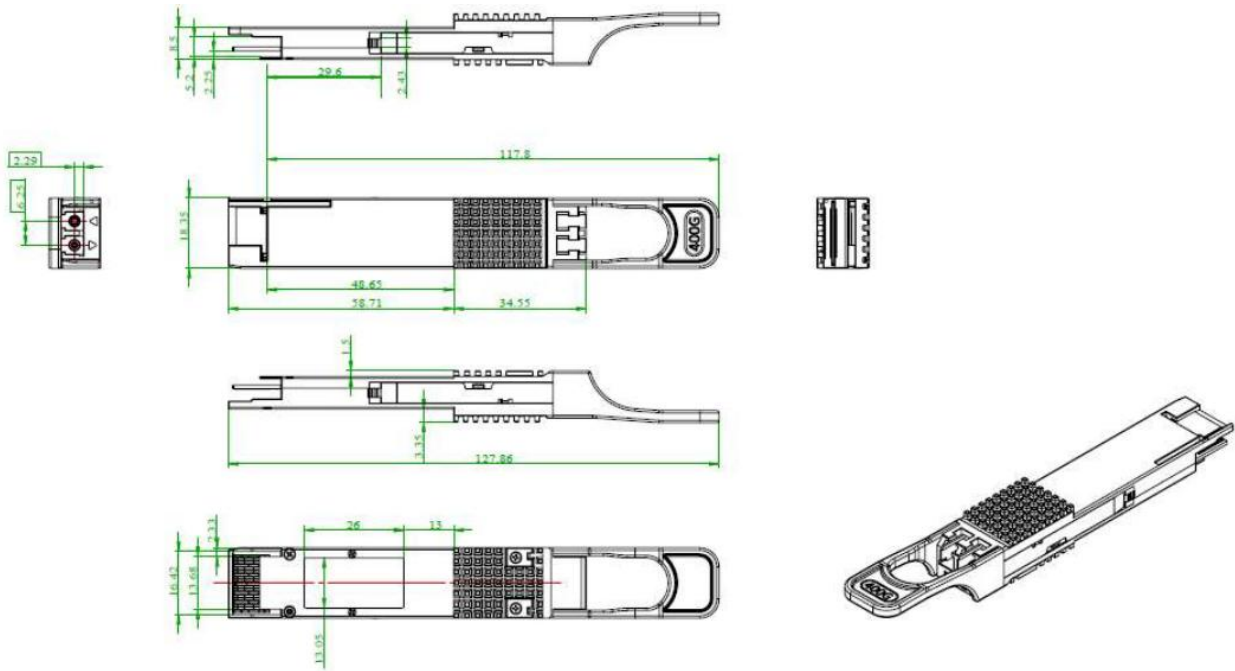


Figure3 Mechanical Outline



## Further Information:

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