

400Gb/s QSFP-DD LR4 1310nm 10km Optical Transceiver

Features

- Maximum Power Consumption 10W
- Case Operating Temperature 0°C to 70°C
- Two Wire Serial Interface with Digital Diagnostic Monitoring
- Class 1 Laser
- Compliant with QSFP-DD MSA HW Rev 5.0 Type 2 Housing with MPO-12 Connector
- Compliant with QSFP-DD CMIS Rev 4.0
- Compliant with EU Directive 2011/65/EU (RoHS Compliant)
- Compliant with IEEE802.3bs Standard: 400GAUI-8 Electrical
- Compliant with IEEE802.3cu Standard: 4x100GBASE-LR1 Optical Interface

Applications

- Data Center Interconnect
- 400G Ethernet
- Enterprise Networking

Description

This product is a 400Gb/s Quad Small Form Factor Pluggable-double density (QSFP-DD) optical module designed for 10km optical communication applications. The product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP-DD Multi- Source Agreement (MSA).

Absolute Maximum Ratings

Table1-Absolute Maximum Ratings						
Parameter	Symbol	Min.	Typical	Max.	Unit	Note
Storage Temperature Range	Ts	-40		85	°C	
Relative Humidity (Non-condensing)	RH	5		95	%	
Supply Voltage	VCC	-0.5		3.6	V	
Control Input Voltage	VI	-0.3		VCC+0.5	V	

Recommended Operating Conditions

Table2-Recommended Operating Conditions						
Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Operating Case Temperature	TOPR	0		70	°C	
Power Supply Voltage	VCC	3.135	3.3	3.465	V	
Instantaneous Peak Current at Hot Plug	ICC_IP			4000	mA	
Sustained Peak Current at Hot Plug	ICC_SP			3300	mA	
Maximum Power Dissipation	PD			10	W	
Maximum Power Dissipation, Low Power Mode	PDLP			1.5	W	
Signaling Rate Per Lane	SRL		53.125		GBd	PAM4
Two Wire Serial Interface Clock Rate				400	kHz	
Power Supply Noise Tolerance (10Hz-10MHz)				66	mV	
Rx Differential Data Output Load			100		Ohm	
Operating Distance		2		10000	m	

Electrical Characteristics Low Speed Signal

Table3-Electrical Characteristics Low Speed Signal						
Parameter	Symbol	Min.	Typical	Max	Unit	Notes
Module Output SCL and SDA	VOL	0		0.4	V	
Module Input SCL and SDA	VIL	-0.3		VCC*0.3	V	
	VIH	VCC*0.7		VCC+0.5	V	
Init Mode, ResetL and ModSelL	VIL	-0.3		0.8	V	
	VIH	2		VCC+0.3	V	
IntL	VOL	0		0.4	V	
	VOH	VCC-0.5		VCC+0.3	V	

Electrical Characteristics High Speed Signal

Table4-Electrical Characteristics High Speed Signal						
Parameter	Symbol	Min	Typical.	Max	Unit	Notes
Transmitter Electrical Characteristics						
Differential Pk-pk Input Voltage Tolerance		900			mV	
Differential Termination Mismatch				10	%	
Single-ended Voltage Tolerance Range		-0.4		3.3	V	
DC Common Mode Voltage		-350		2850	mV	
Receiver Electrical Characteristics						
AC Common-mode Output Voltage (RMS)				17.5	mV	
Differential Output Voltage				900	mV	
Near-end Eye height, Differential		70			mV	
Far-end Eye height, Differential		30			mV	
Far end Pre-cursor Ratio		-4.5		2.5	%	
Differential Termination Mismatch				10	%	
Transition Time (Min, 20% to 80%)		9.5			ps	
DC Common Mode Voltage		-350		2850	mV	

Optical Characteristics

Table5-Optical Characteristics

Parameter	Symbol	Min.	Typical	Max	Unit	Notes
Transmitter Optical Characteristics						
Wavelength	C	1304.5	1311	1317.5	nm	
Side Mode Suppression Ratio	SMSR	30			dB	
Average Launch Power, Each Lane	AOPL	- 1.9		4.8	dBm	1
Outer Optical Modulation Amplitude (OMA _{outer}), Each Lane	TOMA			5	dBm	
Outer Optical Modulation Amplitude (OMA _{outer}), Each Lane: for TDECQ <1.4dB for 1.4<TDECQ<3.4dB	TOMA	1.1 -0.3+TDECQ			dBm	
Transmitter and Dispersion Eye Closure for PAM4(TDECQ), Each Lane	TDECQ			3.4	dB	
Transmitter Eye Closure for PAM4(TECQ)	TECQ			3.4	dB	
TDECQ-TECQ				2.5	dB	
Over/Under-shoot				22	%	
Transmitter Power Excursion				2.8	dBm	
Average Launch Power of OFF Transmitter, Each Lane	TOFF			- 15	dBm	
Extinction Ratio, Each Lane	ER	3.5			dB	
RIN15.6OMA	RIN			- 136	dB/Hz	
Optical Return Loss Tolerance	ORL			15.6	dB	
Transmitter Reflectance	TR			-26	dB	
Transmitter Transition Time	Tt			17	ps	
Receiver Optical Characteristics						
Wavelength	λ C	1304.5	1311	1317.5	nm	
Damage Threshold, Each Lane	AOPD	5.8			dBm	
Average Receive Power, Each Lane	AOPR	-8.2		4.8	dBm	2
Receive Power(OMA _{outer}), Each Lane	OMAR			5	dBm	
Receiver Reflectance	RR			-26	dB	
Receiver Sensitivity(OMA _{outer}), Each Lane for TECQ<1.4dB for 1.4≤TECQ≤3.4dB	SOMA			-6.1 -7.5+TECQ	dBm	
Stressed Receiver Sensitivity(OMA _{outer}), Each Lane	SRS			-4.1	dBm	3
Conditions of Stressed Receiver Sensitivity Test						
Stressed Eye Closure for PAM4(SECQ)			3.4		dB	

Notes:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength.

2. Average receive power, (min) is informative and not the principal indicator of signal strength.
3. Measured with conformance test signal at TP3 for the BER = 2.4×10^{-4} .

Pin Description

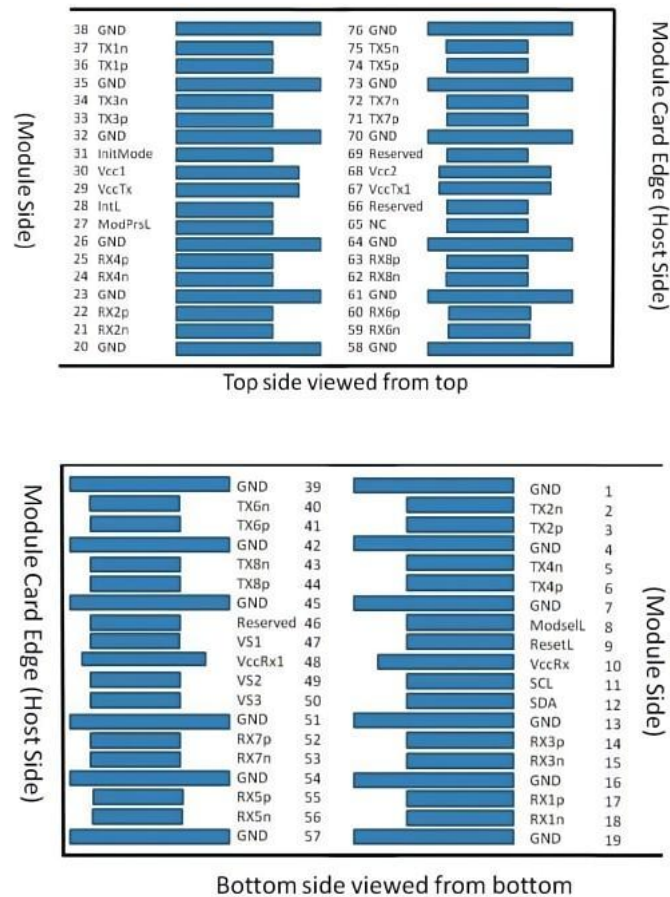


Figure1. Pin Definitions of the Module High Speed Inputs/Outputs

Transceiver Pin Descriptions

Table6-Pin Descriptions

Pin	Logic	Symbol	Description
1		GND	Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input
4		GND	Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input

7		GND	Ground
8	LVTTL-I	ModSelL	Module Select
9	LVTTL-I	ResetL	Module Reset
10		Vcc Rx	+3.3V Power Supply Receiver
11	LVC MOS-I/O	SCL	2-wire serial interface clock
12	LVC MOS-I/O	SDA	2-wire serial interface data
13		GND	Ground
14	CML-O	Rx3p	Receiver Non-Inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output
16	GND	GND	Ground
17	CML-O	Rx1p	Receiver Non-Inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output
19		GND	Ground
20		GND	Ground
21	CML-O	Rx2n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-Inverted Data Output
23		GND	Ground
24	CML-O	Rx4n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-Inverted Data Output
26		GND	Ground
27	LVTTL-O	ModPrsL	Module Present
28	LVTTL-O	IntL/RxLOSL	Interrupt. Optionally configurable as RxLOSL via the management interface (SFF-8636)
29		VccTx	+3.3V Power supply transmitter
30		Vcc1	+3.3V Power supply
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE
32		GND	Ground
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input
35		GND	Ground
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input
38		GND	Ground
39		GND	Ground
40	CML-I	Tx6n	Transmitter Inverted Data Input
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input
42		GND	Ground
43	CML-I	Tx8n	Transmitter Inverted Data Input
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input
45		GND	Ground
46		Reserved	For future use

47		VS1	Module Vendor Specific 1
48		VccRx1	3.3V Power Supply
49		VS2	Module Vendor Specific 2
50		VS3	Module Vendor Specific 3
51		GND	Ground
52	CML-0	Rx7p	Receiver Non-Inverted Data Output
53	CML-0	Rx7n	Receiver Inverted Data Output
54		GND	Ground
55	CML-0	Rx5p	Receiver Non-Inverted Data Output
56	CML-0	Rx5n	Receiver Inverted Data Output
57		GND	Ground
58		GND	Ground
59	CML-0	Rx6n	Receiver Inverted Data Output
60	CML-0	Rx6p	Receiver Non-Inverted Data Output
61		GND	Ground
62	CML-0	Rx8n	Receiver Inverted Data Output
63	CML-0	Rx8p	Receiver Non-Inverted Data Output
64		GND	Ground
65		NC	No Connect
66		Reserved	For future Use
67		VccTx1	3.3V Power Supply
68		Vcc2	3.3V Power Supply
69		Reserved	For future Use
70		GND	Ground
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input
72	CML-I	Tx7n	Transmitter Inverted Data Input
73		GND	Ground
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input
75	CML-I	Tx5n	Transmitter Inverted Data Input
76		GND	Ground

Further Information:

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