400Gb/s QSFP-DD LR8 1310nm 10km Optical Transceiver

Features

- Compliant with IEEE 802.3bs standard:
- -400GBASE-LR8 optical interface
- -400GAUI-8 electrical interface
- Compliant with QSFP-DD MSA HW Rev 3.0with duplex LC connector
- Maximum power consumption 14 W
- Case operating temperature 0°C to 70°
- Two wire serial Interface with digital diagnostic monitoring
- Complies with EU Directive2011/65/EU (RoHS compliant)
- Class 1 Laser

Applications

- 400GBASE-LR8 400G Ethernet
- Data Center

Absolute Maximum Ratings

Table1-Absolute Maximum Ratings

Parameter	Symbols	Min.	Max.	Unit	Notes
Storage Temperature Range	TS	-40	85	℃	
Supply Voltage	Vcc	-0.5	3.6	V	
Relative Humidity (non-condensing)	RH	5	95	%	
Data Input Voltage Differential	ivDip-vDiNi		1	V	
Control Input Voltage	V|	-0.3	Vcc+0.5	V	
Control Output Current	l0	-20	20	mA	

Recommended Operating Conditions

Table2-Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Operating Case Temperature	Topr	0		70	°C	1
Power Supply Voltage	Vcc	3.135	3.3	3.465	V	
Instantaneous peak current at hot Plug	lcc_ip			TBD	mA	
Sustained peak current at hot plug	l(2C_SP			TBD	mA	
Maximum Power Dissipation	Pd			TBD	W	
Maximum Power Dissipation, Low Power Mode	Pdlp			TBD	W	
Signaling Speed per Lane	DRL		26.5625		Gbd	
Control Input Voltage High	VIH	Vcc*0.7		Vcc+0.3	V	
Control Input Voltage Low	VIL	-0.3		Vcc*0.3	V	
Two Wire Serial Interface Clock Rate				400	kHz	
Power Supply Noise				50	mVpp	
Rx Differential Data Output Load			100		Ohm	
Operating Distance		2		10000	m	

Optical Characteristics

Table3-Optical Characteristics

Parameter	Symbol	Min	Typical.	Max	Unit	Notes
Transmitter						
Wavelength LO	λ co	1272.55	1273.55	1274.54	nm	
Wavelength LI	λ c1	1276.89	1277.89	1278.89	nm	

Wavelength L2	λc2	1281.25	1282.26	1283.27	nm	
Wavelength L3	λc3	1285.65	1286.67	1287.68	nm	
Wavelength L4	λc4	1294.53	1295.56	1296.59	nm	
Wavelength L5	λc5	1299.02	1300.06	1301.09	nm	
Wavelength L6	λc6	1303.54	1304.59	1305.63	nm	
Wavelength L7	λc7	1308.09	1309.14	1310.19	nm	
Side Mode Suppression Ratio	SMSR	30			dB	
Total Average Launch Power	AOPt			13.2	dBm	
Average Launch Power, each lane	AOPl	-2.8		5.3	dBm	1
Outer Optical Modulation Amplitude (OMA_{outer}), each Lane	Toma	0.2		5.7	dBm	
Difference in Launch Power between any two Lanes (OMA_{outer})	DT_OMA			4	db	
Launch Power in OMA_{outer} minus TDECQ, each lane for ER＞4.5dB	TomA-TDECQ	-1.2			dBm	
Launch Power in OMAouter minus TDECQ, each lane for ER＜4.5dB	Tqma-tdecq	-1.1			dBm	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each lane	TEDCQ			3.3	dB	
Average Launch Power of OFF Transmitter, each lane	Toff			-30	dBm	
Extinction Ratio	ER	3.5			dB	
rin151oma	RIN			-132	dB/Hz	
Optical Return Loss Tolerance	ORL			15.1	dB	
Transmitter Reflectance	Tr			-26	dB	2
Receiver						
Wavelength LO	λco	1272.55	1273.55	1274.54	nm	
Wavelength LI	λc1	1276.89	1277.89	1278.89	nm	
Wavelength L2	λc2	1281.25	1282.26	1283.27	nm	
Wavelength L3	λc3	1285.65	1286.67	1287.68	nm	
Wavelength L4	λc4	1294.53	1295.56	1296.59	nm	
Wavelength L5	λc5	1299.02	1300.06	1301.09	nm	
Wavelength L6	λc6	1303.54	1304.59	1305.63	nm	
Wavelength L7	λc7	1308.09	1309.14	1310.19	nm	
Damage Threshold, each Lane	aopd	6.3			dBm	
Average Receive Power, each Lane	aopr	-9.1		5.3	dBm	
Receive Power (OMA_{outer}), each Lane	omar			5.7	dBm	
Difference in Receive Power between any two Lanes (OMA_{outer})	Droma			4.5	dB	
Receiver Reflectance	RR			-26	dB	

Receiver Sensitivity (OMA_{outer}), each Lane	Soma			-7.1	dBm	1
Stressed Receiver Sensitivity (OMA_{outer})， each Lane	SRS			-4.7	dBm	2

Notes:

1 .Average launch power, each lane (min) is informative and not the principal indicator of signal strength

2.Transmitter reflectance is defined looking into the transmitter

3 .Receiver sensitivity (OMA_{outer}), each lane (max) is informative and is defined for a transmitter with SECQ of 0.9 dB

4.Measured with conformance test signal at TP3 for the BER = 2.4x10-4

Electrical Characteristics

Table4-Electrical Characteristics

Parameter	Symbol	Min.	Typical	Max	Unit	Notes
Transmitter						
Differential pk-pk input Voltage tolerance		900			mV	
Differential termination mismatch				10	%	
Single-ended voltage tolerance range		-0.4		3.3	V	
DC common mode Voltage		-350		2850	mV	
Receiver						
AC common-mode output Voltage (RMS）				17.5	mV	
Differential output Voltage				900	mV	
Near-end Eye height,differential		70			UI	
Far-end Eye height, differential		30			UI	
Far end pre-cursor ratio				2.5	%	
Differential Termination Mismatch				10	%	
Transition Time (min, 20% to80%)		9.5			ps	
DC common mode Voltage		-350		2850	mV	

Electrical Specification Low Speed Signal (compliant with QSFP-DD HW Rev 3.0)

Parameter	Symbols	Min.	Max	Unit	Notes
Module Output SC Land SDA	Vol	0	0.4	V	
Module Input SCL and SDA	V0H	Vcc-0.5	Vcc+0.3	V	
	V|L	-0.3	Vcc*0.3	V	
InitMode, ResetL and ModSelL	V|H	V/.7	Vcc+0.5	V	
	V|L	-0.3	0.8	V	
IntL	VOL	0	0.4	V	
	VOH	VCC-0.5	VCC+0.3	V	

Table5-Electrical Characteristics

Parameter	Range	Accuracy.	Unit	Calibration
Temperature	0 to 70	±3	°C	Internal
Voltage	0 to VCC	0. 1	V	Internal
Tx Bias Current (each Lane)	0 to 100	10%	mA	Internal
Tx Output Power (each Lane)	-3.5 to +5.3	±3dB	dBm	Internal
Rx Receive Power (each Lane)	-9.1 to +5.3	±3dB	dBm	Internal

Pin Description

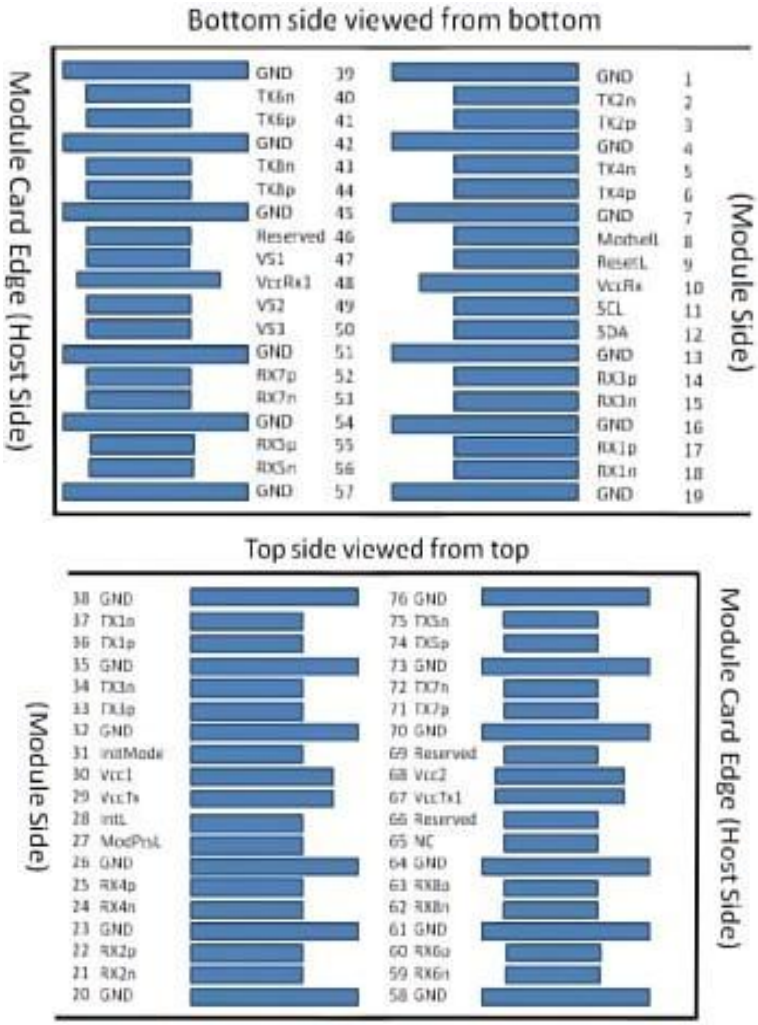


Figure 1 Pin view

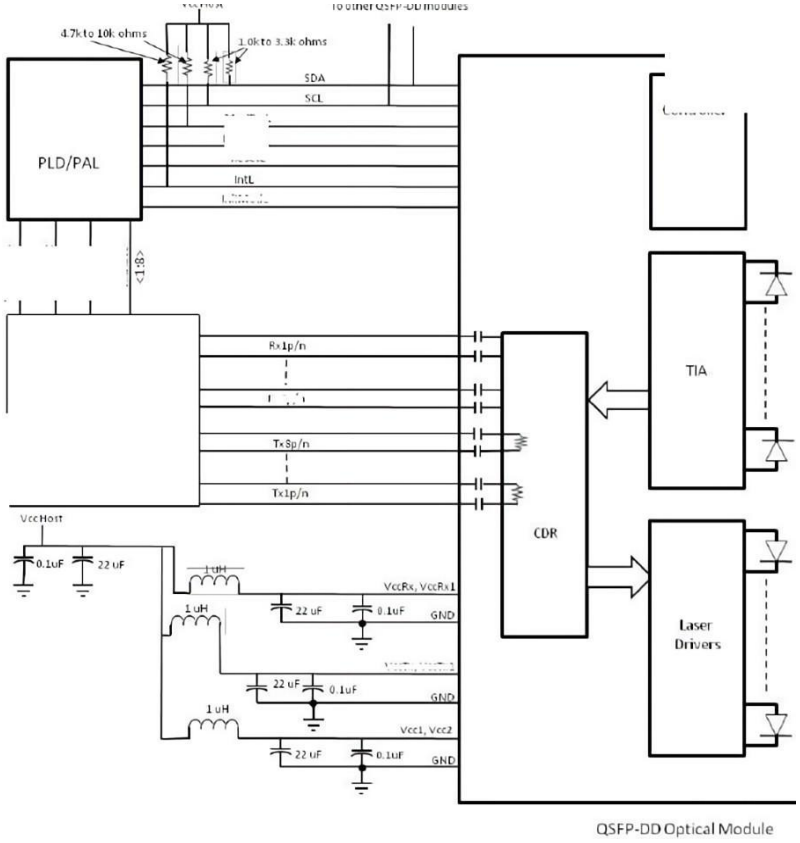
Pin Function Definitions

Table6-Pin Descriptions

Pin	Logic	Symbol	Description
1		GND	Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input
4		GND	Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input
7		GND	Ground
8	LVTTL-I	ModSelL	Module Select
9	LVTTL-I	ResetL	Module Reset
10		Vcc Rx	+3.3V Power Supply Receiver
11	LVCMOS-I/O	SCL	2-wire serial interface clock
12	LVCMOS-I/O	SDA	2-wire serial interface data
13		GND	Ground
14	CML-O	Rx3p	Receiver Non-Inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output
16	GND	GND	Ground
17	CML-O	Rx1p	Receiver Non-Inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output
19		GND	Ground
20		GND	Ground
21	CML-O	Rx2n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-Inverted Data Output
23		GND	Ground
24	CML-O	Rx4n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-Inverted Data Output
26		GND	Ground
27	LVTTL-O	ModPrsL	Module Present
28	LVTTL-O	IntL/RxLOSL	Interrupt. Optionally configurable as RxLOSL via the management interface (SFF-8636)
29		VccTx	+3.3V Power supply transmitter
30		Vcc1	+3.3V Power supply
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE
32		GND	Ground
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input
35		GND	Ground

36	CML-I	Tx1p	Transmitter Non-Inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input
38		GND	Ground
39		GND	Ground
40	CML-I	Tx6n	Transmitter Inverted Data Input
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input
42		GND	Ground
43	CML-I	Tx8n	Transmitter Inverted Data Input
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input
45		GND	Ground
46		Reserved	For future use
47		VS1	Module Vendor Specific 1
48		VccRx1	3.3V Power Supply
49		VS2	Module Vendor Specific 2
50		VS3	Module Vendor Specific 3
51		GND	Ground
52	CML-O	Rx7p	Receiver Non-Inverted Data Output
53	CML-O	Rx7n	Receiver Inverted Data Output
54		GND	Ground
55	CML-O	Rx5p	Receiver Non-Inverted Data Output
56	CML-O	Rx5n	Receiver Inverted Data Output
57		GND	Ground
58		GND	Ground
59	CML-O	Rx6n	Receiver Inverted Data Output
60	CML-O	Rx6p	Receiver Non-Inverted Data Output
61		GND	Ground
62	CML-O	Rx8n	Receiver Inverted Data Output
63	CML-O	Rx8p	Receiver Non-Inverted Data Output
64		GND	Ground
65		NC	No Connect
66		Reserved	For future Use
67		VccTx1	3.3V Power Supply
68		Vcc2	3.3V Power Supply
69		Reserved	For future Use
70		GND	Ground
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input
72	CML-I	Tx7n	Transmitter Inverted Data Input
73		GND	Ground
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input
75	CML-I	Tx5n	Transmitter Inverted Data Input
76		GND	Ground

Recommended QSFP-DD Host Board Schematic



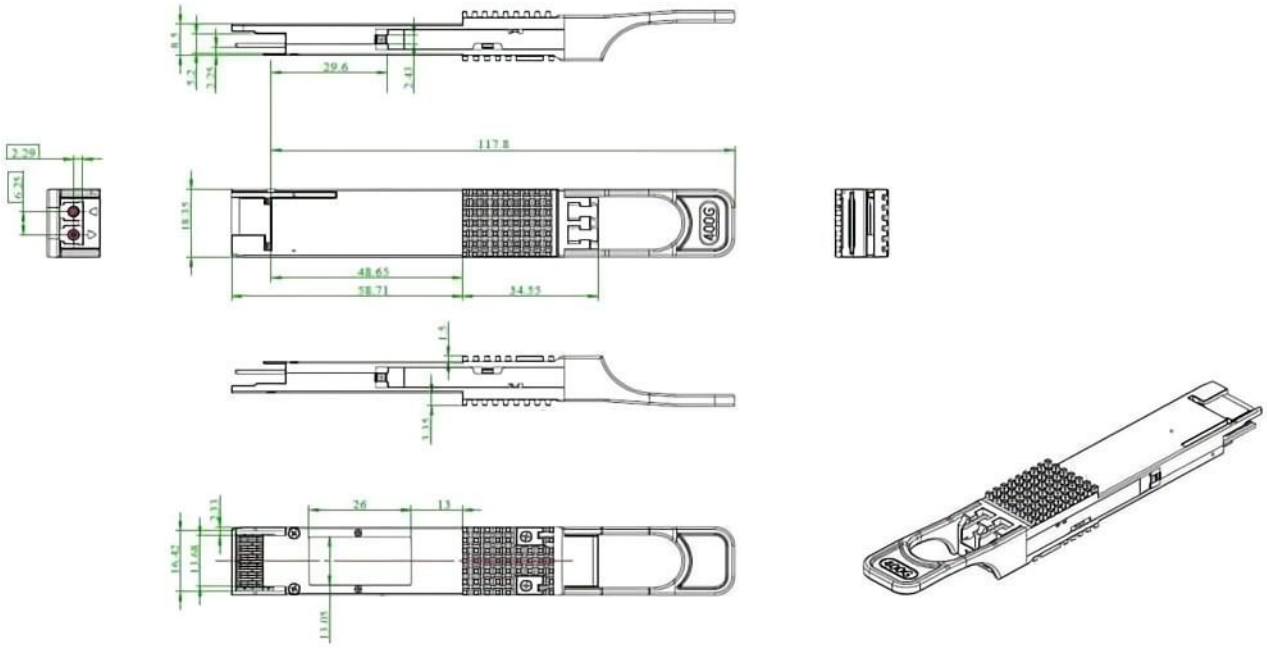
Timing for Soft Control and Status Functions

Parameter	Symbols	Min.	Max.	Unit	Notes
Mgmtlnit Duration			2000	ms	
ResetL Assert Time	t_reset_init	10		μs	
IntL Assert Time	ton_IntL		200	ms	
IntL Deassert Time	toff_IntL		500	μs	
Rx LOS Assert Time (Fast Mode)	ton_losf		100	ms	
Tx Fault Assert Time	ton_Txfault		200	ms	
Flag Assert Time	ton_flag		200	ms	
Mask Assert Time	ton_mask		100	ms	
Mask Deassert Time	toff_mask		100	ms	
Application or Rate Select Change Time	t_ratesel		N/A	ms	1

I/O Timing for Squelch and Disable

Parameter	Symbols	Max.	Unit	Notes
Rx Squelch Assert Time	ton_Rxsq	15	ms	
Rx Squelch Deassert Time	toff_Rxsq	15	ms	
Tx Squelch Assert Time	ton_Txsq	400	ms	1
Tx Squelch Deassert Time	toff_Txsq	400	ms	1
Tx Disable Assert Time (Fast Mode)	ton_Txdisf	100	ms	
Tx Disable Deassert Time(Fast Mode)	toff_Txdisf	400	ms	
Rx Output Disable Assert Time	ton_Rxdis	100	ms	
Rx Output Disable Deassert Time	toff_Rxdis	100	ms	
Squelch Disable Assert Time	ton_sqdis	100	ms	
Squelch Disable Deassert Time	toff_sqdis	100	ms	

Mechanical Dimensions



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