# 100Gb/s and 112Gb/s QSFP28 LR4 1310nm 20km Optical Transceiver

## Features

- Hot pluggable QSFP28 MSA form factor
- Lane data rate of 25.78125Gb/s,27.953Gb/s
- Up to 20km reach for G.652 SMF
- Single +3.3V power supply
- Operating case temperature: 0℃ ~70℃
- Transmitter: cooled 4x25Gb/s LAN WDM DFB TOSA
- Receiver: 4x25Gb/s PIN ROSA
- Maximum power consumption 3.5W
- 4x28G Electrical Serial Interface (CEI-28G-VSR)
- Duplex LC receptacle
- RoHS-6 compliant

## Applications

- 100GBASE-LR4 Ethernet Links
- OTN OTU4 4I1-9D1F

## General Description

This product is a 100Gb/s transceiver module designed for optical communication applications compliant to 100GBASE-LR4 of the IEEE P802.3ba and OTU4 4I1-9D1F standard. The module converts 4 input channels of 25Gb/s electrical data to 4 channels of LAN WDM optical signals and then multiplexes them into a single channel for 100Gb/s optical transmission. Reversely on the receiver side, the module de-multiplexes a 100Gb/s optical input into 4 channels of LAN WDM optical signals and then converts them to 4 output channels of electrical data.

The central wavelengths of the 4 LAN WDM channels are 1295.56, 1300.05, 1304.58 and 1309. 14nm as members of the LAN WDM wavelength grid defined in IEEE 802.3ba. The high performance cooled LAN WDM DFB transmitters and high sensitivity PIN receivers provide superior performance for 100Gigabit Ethernet applications up to 20km links and compliant to optical interface with IEEE802.3ba Clause 88 100GBASE-LR4 requirements.

The product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP+ Multi-Source Agreement (MSA). It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference.

## Functional Description

The transceiver module receives 4 channels of 25Gb/s electrical data, which are processed by a 4-channel Clock and Data Recovery (CDR) IC that reshapes and reduces the jitter of each electrical signal. Subsequently, each of 4 DML laser driver IC's converts one of the 4 channels of electrical signals to an optical signal that is transmitted from one of the 4 cooled DML lasers which are packaged in the Transmitter Optical Sub-Assembly (TOSA). Each laser launches the optical signal in specific wavelength specified in IEEE802 .3ba 100GBASE-LR4 requirements. These 4-lane optical signals will be optically multiplexed into a single fiber by a 4-to- 1 optical WDM MUX. The optical output power of each channel is maintained constant by an automatic power control (APC) circuit. The transmitter output can be turned off by TX_DIS hardware signal and/or 2-wire serial interface.

The receiver receives 4-lane LAN WDM optical signals. The optical signals are de-multiplexed by a 1-to-4 optical DEMUX and each of the resulting 4 channels of optical signals is fed into one of the 4 receivers that are packaged into the Receiver Optical Sub-Assembly (ROSA). Each receiver converts the optical signal to an electrical signal. T he regenerated electrical signals are re-timed and de-jittered and amplified by the RX portion of the 4-channel CDR. The re-timed 4-lane output electrical signals are compliant with IEEE CAUI-4 interface requirements. In addition, each received optical signal is monitored by the DOM section. The monitored value is reported through the 2- wire serial interface. If one or more received optical signal is weaker than the threshold level, RX_LOS hardware alarm will be triggered. A single +3.3V power supply is required to power up this product. Both power supply pins VccTx and VccRx are internally connected and should be applied concurrently. As per MSA specifications the module offers 7 low speed hardware control pins (including the 2-wire serial interface): ModSelL, SCL, SDA, ResetL, LPMode, ModPrsL and IntL.

Module Select (ModSelL) is an input pin. When held low by the host, this product responds to 2-wire serial communication commands. The ModSelL allows the use of this product on a single 2-wire interface bus – individual ModSelL lines must be used.

Serial Clock (SCL) and Serial Data (SDA) are required for the 2-wire serial bus communication interface and enable the host to access the QSFP28 memory map.

The ResetL pin enables a complete reset, returning the settings to their default state, when a low level on the ResetL pin is held for longer than the minimum pulse length. During the execution of a reset the host shall disregard all status bits until it indicates a completion of the reset interrupt. The product indicates this by posting an IntL (Interrupt) signal with the Data_ Not_ Ready bit negated in the memory map. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a resetLow Power Mode (LPMode) pin is used as TX disable. If the LPMode pin is in the high state, the modulor will tune off the Laser.

Module Present (Mod PrsL) is a signal local to the host board which, in the absence of a product, is normally pulled up to the host Vcc. When the product is inserted into the connector, it completes the path to ground through a resistor on the host board and asserts the signal. ModPrsL then indicates its present by setting ModPrsL to a "Low" state.

Interrupt (IntL) pin is used as RX-LOS. When "Low", it indicates a RX-LOS assert. Other alarm asserting does not go though IntL pin.

## Absolute Maximum Ratings

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

**Table1-Absolute Maximum Ratings**

| Parameter | Symbols | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| Storage Temperature | Ts | -40 | 85 | ℃ | |
| Operating Case Temperature | TOP | 0 | 70 | ℃ | |
| Power Supply Voltage | VCC | -0.5 | 3.6 | V | |
| Relative Humidity (non-condensation) | RH | 0 | 85 | % | |
| Damage Threshold, each Lane | THd | 5.5 | | dBm | |

## Recommended Operating Conditions

**Table2-Recommended Operating Conditions**

| Parameter | Symbols | Min. | Typical | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| Operating Case Temperature | TOP | 0 | | 70 | ℃ | |
| Power Supply Voltage | VCC | 3.135 | 3.3 | 3.465 | V | |
| Data Rate, each Lane | | | 25.78 | | Gb/s | |
| Control Input Voltage High | | 2 | | VCC | V | |
| Control Input Voltage Low | | 0 | | 0.8 | V | |
| Link Distance with G.652 | D | 0.002 | | 20 | km | |

## Optical，Characteristic

**Table3-Transmitter Operating Characteristic-Optical**

| QSFP28 100GBASE-LR4 | | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbols** | **Min.** | **Typical** | **Max.** | **Unit** | **Notes** |
| Signaling Speed per Channel | | | 25.78125 | | Gbps | |
| Lane Wavelength | L0 | 1294.53 | | 1296.59 | nm | |
| | L1 | 1299.02 | | 1301.09 | nm | |
| | L2 | 1303.54 | | 1305.63 | nm | |
| | L3 | 1308.09 | | 1310. 19 | nm | |
| Transmitter | | | | | | |
| Side Mode Suppression Ratio | SMSR | 30 | | | dB | 2 |
| Total Average Launch Power | PT | | | 10.5 | dBm | |
| Average Launch Power, each Lane | PAVG | - 1.0 | | 4.5 | dBm | |
| OMA, each Lane | POMA | -0.5 | | 4.5 | dBm | |
| Difference in Launch Power between any Two Lanes(OMA) | Ptx,diff | | | 5 | dB | |

| | | | | | | |
|---|---|---|---|---|---|---|
| Launch Power in OMA minus Transmitter and Dispersion Penalty (TDP), each Lane | | -2.3 | | | dBm | |
| TDP, each Lane | TDP | | | 2.2 | dB | |
| Extinction Ratio | ER | 4 | | | dB | |
| RIN20OMA | RIN | | | - 130 | dB/Hz | |
| Optical Return Loss Tolerance | TOL | | | 20 | dB | |
| Transmitter Reflectance | RT | | | - 12 | dB | |
| Eye Mask{X1, X2, X3, Y1, Y2, Y3} | | {0.25, 0.4, 0.45, 0.25, 0.28, 0.4} | | | | 1 |
| Average Launch Power OFF Transmitter, each Lane | $P_{off}$ | | | -30 | dBm | |
| **Receiver** | | | | | | |
| Signaling Speed per Channel | | | 25.78125 | | Gbps | |
| Lane Wavelength | L0 | 1294.53 | | 1296.59 | nm | |
| | L1 | 1299.02 | | 1301.09 | nm | |
| | L2 | 1303.54 | | 1305.63 | nm | |
| | L3 | 1308.09 | | 1310. 19 | nm | |
| Total Average Receive Power | | | | 10.5 | dBm | |
| Average Receive Power, each Lane | | | | 4.5 | dBm | |
| Receive Power (OMA), each Lane | | | | 4.5 | dBm | |
| Receiver Sensitivity (OMA), each Lane | SEN | | | -9.5 | dBm | 2 |
| Stressed Receiver Sensitivity (OMA), each Lane | | | | -6.8 | dBm | |
| Difference in Receive Power between any Two Lanes (OMA) | Prx,diff | | | 5.5 | dB | |
| LOS Assert | LOSA | -25 | | | dBm | |
| LOS De-assert | LOSD | | | - 13 | dBm | |
| LOS Hysteresis | LOSH | 0.5 | | 6 | dB | |

Notes:

1.Compliant to IEEE 802.3ba.

2.Measured with conformance test signal at receiver input for BER = 1x $10^{-12}$.

| QSFP28 OTU4 | | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbols** | **Min.** | **Typical** | **Max.** | **Unit** | **Notes** |
| Signaling Speed per Channel | | | 27.95 | | Gbps | |
| Lane Wavelength | L0 | 1294.53 | | 1296.59 | nm | |
| | L1 | 1299.02 | | 1301.09 | nm | |
| | L2 | 1303.54 | | 1305.63 | nm | |
| | L3 | 1308.09 | | 1310. 19 | nm | |
| **Transmitter** | | | | | | |
| Side Mode Suppression Ratio | SMSR | 30 | | | dB | |

| | | | | | | |
|---|---|---|---|---|---|---|
| Total Average Launch Power | PT | | | 10 | dBm | |
| Average Launch Power, each Lane | PAVG | 0 | | 4 | dBm | |
| Channel Power Difference | Pout,diff | | | 5 | dB | |
| Extinction Ratio | ER | 4 | | 6.5 | dB | |
| Optical Return Loss Tolerance | TOL | | | 20 | dB | |
| Transmitter Reflectance | RT | | | -12 | dB | |
| Average Launch Power OFF Transmitter, each Lane | Poff | | | -30 | dBm | |
| Receiver | | | | | | |
| Signaling Speed per Channel | | | 27.95 | | Gbps | |
| Lane Wavelength | L0 | 1294.53 | | 1296.59 | nm | |
| | L1 | 1299.02 | | 1301.09 | nm | |
| | L2 | 1303.54 | | 1305.63 | nm | |
| | L3 | 1308.09 | | 1310. 19 | nm | |
| Total Average Receive Power | | | | 10.5 | dBm | |
| Average Receive Power, each Lane | | | | 4 | dBm | |
| Receiver Sensitivity , each Lane | SEN | | | -9.0 | dBm | 1 |
| Total Average Launch Power | PIN | | | 10 | dBm | |
| Difference in Receive Power between any Two Lanes(OMA) | Prx,diff | | | 5.5 | dB | |
| LOS Assert | LOSA | -25 | | | dBm | |
| LOS De-assert | LOSD | | | - 13 | dBm | |
| LOS Hysteresis | LOSH | 0.5 | | 6 | dB | |

Notes:

1. Specified at a BER of 10-6(pre-FEC), per ITU-T G.sup39.

## Electrical Characteristic

The following electrical characteristics are defined over the Recommended Operating Environment unless otherwise specified.

| Parameter | Symbols | Min. | Typical | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| Power Consumption | | | | 3.5 | W | |
| Supply Current | Icc | | | 1. 12 | A | |
| Transmitter (each Lane) | | | | | | |
| Differential Input Voltage Swing | Vin,pp | | | 900 | mVpp | |
| Differential Input Impedance | Zin | 90 | 100 | 1 10 | Ohm | |
| Receiver (each Lane) | | | | | | |
| Differential Output Voltage Swing | Vout,pp | 100 | | 400 | mVpp | 1 |
| | | 300 | | 600 | | |
| | | 400 | | 800 | | |
| | | 600 | | 1200 | | |
| Differential Output Impedance | Zout | 90 | 100 | 1 10 | Ohm | |

Notes:

1. Output voltage is settable in 4 discrete ranges via I2C. Default range is 400 – 800mV.

## Digital Diagnostic Functions

The following digital diagnostic characteristics are defined over the Recommended Operating Environment unless otherwise specified.

It is compliant to SFF-8436.

| Parameter | Symbols | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| Temperature monitor absolute error | DMI_Temp | -5 | 5 | ℃ | Over operating temperature range |
| Supply voltage monitor absolute error | DMI _VCC | -3% | 3% | V | Over full operating range |
| Channel RX power monitor absolute error | DMI_RX_Ch | -2 | 2 | dB | |
| Channel Bias current monitor | DMI_Ibias_Ch | - 10% | 10% | mA | Ch 1~Ch4 |
| Channel TX power monitor absolute error | DMI_TX_Ch | -2 | 2 | dB | |

## Transceiver Block Diagram

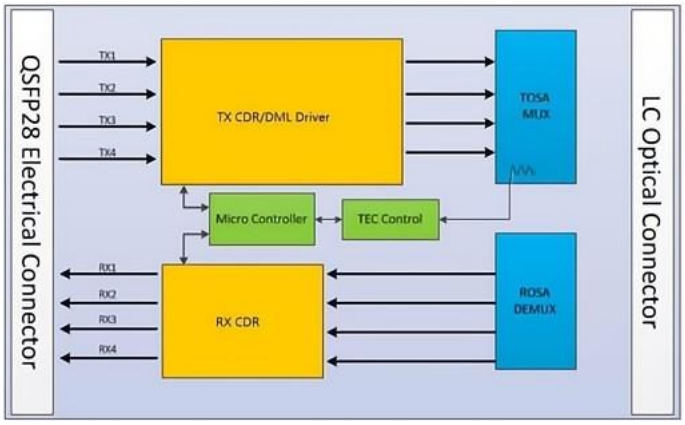


Figure 1 – Transceiver Block Diagram

## Pin Description

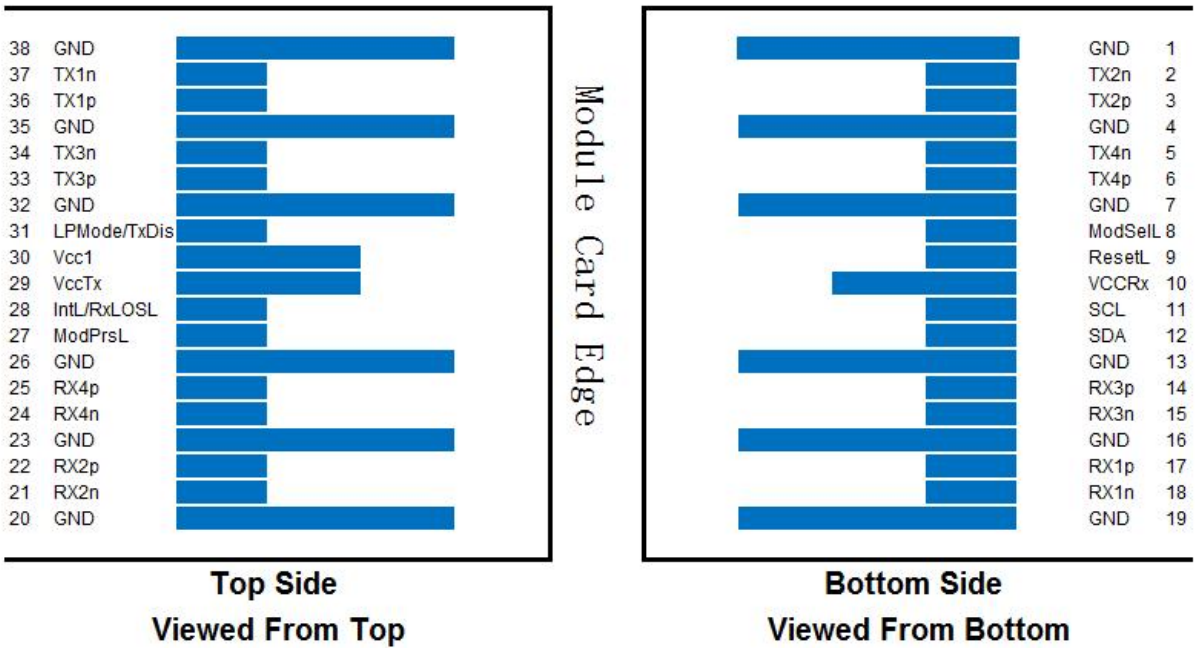


Figure 2 Pin view

## Pin Function Definitions

| Pin | Symbols | Logic | Description | Notes |
|---|---|---|---|---|
| 1 | GND | | Ground | 1 |
| 2 | Tx2n | CML-I | Transmitter Inverted Data Input | |
| 3 | Tx2p | CML-I | Transmitter Non-Inverted Data Input | |
| 4 | GND | | Ground | 1 |
| 5 | Tx4n | CML-I | Transmitter Inverted Data Input | |
| 6 | Tx4p | CML-I | Transmitter Non-Inverted Data Input | |
| 7 | GND | | Ground | |
| 8 | ModSelL | LVTTL-I | Module Select | |
| 9 | ResetL | LVTTL-I | Module Reset | |
| 10 | Vcc Rx | | +3.3V Power Supply Receiver | 2 |
| 11 | SCL | LVCOMS-I/O | 2-wire serial interface clock | |
| 12 | SDA | LVCOMS-I/O | 2-wire serial interface data | |
| 13 | GND | | Ground | |
| 14 | Rx3p | CML-O | Receiver Non-Inverted Data Output | |
| 15 | Rx3n | CML-O | Receiver Inverted Data Output | |
| 16 | GND | | Ground | 1 |
| 17 | Rx1p | CML-O | Receiver Non-Inverted Data Output | |
| 18 | Rx1n | CML-O | Receiver Inverted Data Output | 1 |

| | | | | |
|---|---|---|---|---|
| 19 | GND | | Ground | 1 |
| 20 | GND | | Ground | |
| 21 | Rx2n | CML-O | Receiver Inverted Data Output | |
| 22 | Rx2p | CML-O | Receiver Non-Inverted Data Output | |
| 23 | GND | | Ground | |
| 24 | Rx4n | CML-O | Receiver Inverted Data Output | |
| 25 | Rx4p | CML-O | Receiver Non-Inverted Data Output | |
| 26 | GND | | Ground | 1 |
| 27 | ModPrsL | LVTTL-O | Module Present | |
| 28 | IntL | LVTTL-O | Interrupt | |
| 29 | VccTx | | +3.3V Power supply transmitter | 2 |
| 30 | Vcc1 | | +3.3V Power supply | 2 |
| 31 | LPMode | LVTTL-I | Low Power Mode | |
| 32 | GND | | Ground | 1 |
| 33 | Tx3p | CML-I | Transmitter Non-Inverted Data Input | |
| 34 | Tx3n | CML-I | Transmitter Inverted Data Input | |
| 35 | GND | | Ground | 1 |
| 36 | Tx1p | CML-I | Transmitter Non-Inverted Data Input | |
| 37 | Tx1n | CML-I | Transmitter Inverted Data Input | |
| 38 | GND | | Ground | 1 |

Notes:

1. GND is the symbol for signal and supply (power) common for QSFP28 modules. All are common within the QSFP28 module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.

2.VccRx, Vcc1 and VccTx are the receiver and transmitter power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown in Figure 4 below. Vcc Rx, Vcc1 and Vcc Tx may be internally connected within the QSFP28 transceiver module in any combination. The connector pins are each rated for a maximum current of 1000mA.

## Recommended Power Supply Filter

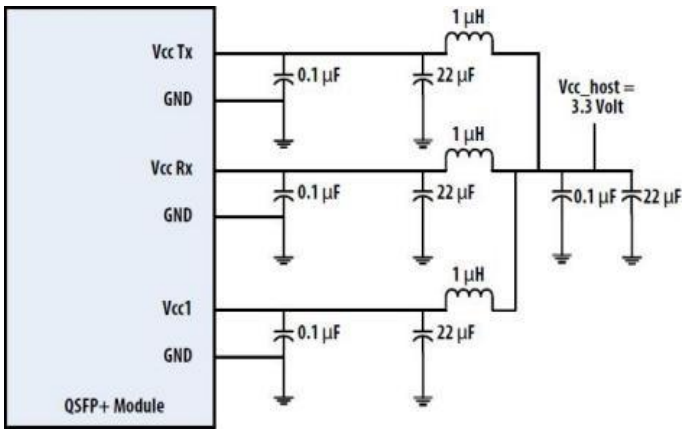


Figure 3 – Recommended Power Supply Filter

## Mechanical Dimensions

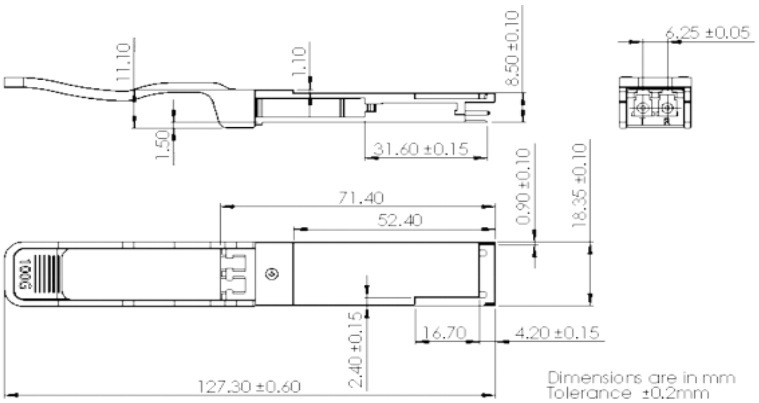


Figure 4 – Mechanical Outline

## ESD

This transceiver is specified as ESD threshold 1kV for high speed data pins and 2kV for all other electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

## Laser Safety

This is a Class 1 Laser Product according to EN 60825-1:2014. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007)

Caution: Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

## Further Information:


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## Disclaimer

1. We are committed to continuous product improvement and feature upgrades, and the contents contained in this manual are subject to change without notice.

2. Nothing herein should be construed as constituting an additional warranty.

3. NADDOD assumes no responsibility for the use or reliability of equipment or software not provided by NADDOD.