40Gb/s QSFP+ LR4 1310nm 10km Optical Transceiver

Features

- Compliant to the industry standard SFF-8436 QSFP+ Transceiver Specification
- QSFP+ MSA compliant
- Up to 11.2Gb/s data rate per wavelength
- 4 CWDM lanes MUX/DEMUX design
- Up to 10km transmission on single mode fiber (SMF)
- Operating case temperature: 0 to 70℃
- Maximum power consumption 3.5W
- LC duplex connector
- ROHS compliant

Applications

- 40GBASE-LR4 Ethernet Links
- Client-side 40G Telecom connections

Compliance

- IEEE802.3ba 40GBASE-LR4
- SFF-8436 QSFP Specification

Description

QSFP-40G-LR4 Transceiver is a high performance, cost effective module for serial optical data communication applications to 41.5Gb/s.The Transceiver is designed to 40GBASE-LR4 of the IEEE P802.3ba standard for 10km links.

The module converts 4 inputs channels (ch) of 10Gb/s electrical data to 4 CWDM optical signals, and multiplexes them into a single channel for 40Gb/s optical transmission. Reversely, on the receiver side, the module optically de-multiplexes a 40Gb/s input into 4 CWDM channels signals, and converts them to 4 channel output electrical data.

The central wavelengths of the 4 CWDM channels are 1271, 1291, 1311 and 1331nm as members of the CWDM wavelength grid defined in ITU-T G.694.2. It contains a duplex LC connector for the optical interface and a 38-pin connector for the electrical interface.

To minimize the optical dispersion in the long-haul system, single-mode fiber (SMF) has to be applied in this module.

Absolute Maximum Ratings

Table1-Absolute Maximum Ratings

Parameter	Symbols	Min.	Typical	Max.	Unit	Notes
Storage Temperature	TSTG	-40		+85	°C	
3.3V Supply Voltage	VCC	-0.5		+3.6	V	
Operating Temperature	Top	0		70		
Operating Relative Humidity	RH	0		85	%	

Recommended Operating Conditions

Table2-Recommended Operating Conditions

Parameter	Symbols	Min.	Typical	Max.	Unit	Notes
Operating Case Temperature	Tc	0		+70	°C	
3.3V Supply Voltage	VCC	3.135	3.3	3.465	V	
Data Rate			41.25		Gbps	
Receiver Differential Data Output Load		90	100	110	Ohms	
Logic Input Voltage High	Vih	2		Vcc+0.3	V	
Logic Input Voltage Low	Vil	-0.3		0.8	V	
Two wire Serial Interface Clock Rate			100	400	KHz	
Power Noise and Ripple				50	mVpp	
Fiber Length				10	km	
Power Dissipation	PD			3.5	W	
Transceiver Power Supply Current				1008	mA	

Electrical Characteristic

Table3-Electrical Characteristic

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Transmitter						
Wavelength λ 0	λ 0	1264.5		1277.5	nm	
Wavelength λ 1	λ 1	1284.5		1297.5	nm	
Wavelength λ 2	λ 1	1304.5		1317.5	nm	
Wavelength λ 3	λ 3	1324.5		1337.5	nm	
Side-Mode Suppression Ratio	SMSR	30			dB	
Spectral width	SW	-7		1.0	nm	
Average power, each lane(EOL)	TXP	3.5		2.3	dBm	
Extinction Ratio	ER	1324.5			dB	
Optical Modulation Amplitude	OMA	-4		3.5	dBm	
Launch Power in OMA minus TDP, each lane		-4.8			dBm	
Difference in Power between any two lanes				6.5	dB	
Optical Return Loss Tolerance				20	dB	
Average launch power of OFF transmitter, per lane				-30	dBm	
Transmitter Eye Mask Definition {X1, X2, X3, Y1, Y2, Y3}			{0.25,0.4, 0.45,0.25, 0.28,0.4}			
Eye Mask Margin	EMM	5			%	
Receiver						
Wavelength λ 0	λ 0	1264.5		1277.5	nm	
Wavelength λ 1	λ 1	1284.5		1297.5	nm	
Wavelength λ 2	λ 2	1304.5		1317.5	nm	
Wavelength λ 3	λ 3	1324.5		1337.5	nm	
Saturation power（EOL）		2.3			dBm	
Max Input power		2.3			dBm	
Sensitivity（OMA EOL）,each lane				-11.5	dBm	
Stressed Receiver Sensitivity(OMA、EOL) ,each lane				-9.6	dBm	
Receiver Reflectance				-26	dBm	

Rx_Loss assert	LOSA	-30			dBm	
Rx_Loss De_assert	LOSD			-12	dB	
LOS Hysteresis		0.5				
Rx output squelch function			Yes			
Rx LOS in signal or RSSI			RSSI			

Pin Description

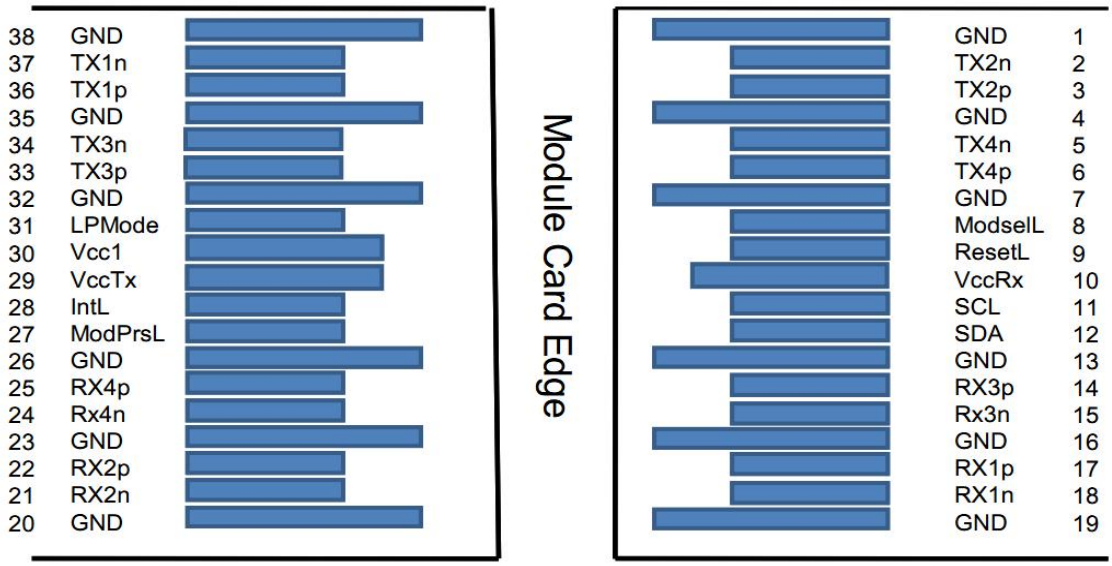

Figure 1 Pin view

Pin Function Definitions

Table4-Pin Function Definitions

Pin	Symbol	Description	Note
1	GND	Ground	1
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data Input	
4	GND	Ground	1
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data Input	
7	GND	Ground	1

8	ModSelL	Module Select	
9	ModSelL	Module Select	
10	Vcc Rx	+3.3V Power Supply Receiver	2
11	SCL	2-wire serial interface clock	
12	SDA	2-wire serial interface data	
13	GND	Ground	1
14	Rx3p	Receiver Non-Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	
16	GND	Ground	1
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1p	Receiver Inverted Data Output	
19	GND	Ground	1
20	GND	Ground	1
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Ground	
24	Rx4n	Receiver Inverted Data Output	
25	Rx4p	Receiver Non-Inverted Data Output Ground	
26	GND	Ground	1
27	ModPrsL	Module Present	
28	IntL	Interrupt	
29	Vcc Tx	+3.3V Power supply transmitter	2
30	Vcc1	+3.3V Power supply	2
31	LPMode	Low Power Mode	
32	GND	Ground	1
33	Tx3p	Transmitter Non-Inverted Data Input	
34	Tx3n	Transmitter Inverted Data Input	
35	GND	Ground	1
36	Tx1p	Transmitter Non-Inverted Data Input	
37	Tx1n	Transmitter Inverted Data Input	
38	GND	Ground	1

Notes:

[1] GND is the symbol for signal and supply (power) common for the QSFP+ module. All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

[2] Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently.Recommended host board power supply filtering is shown in Figure 3. Vcc Rx Vcc1 and VccTx may be internally connected within the QSFP+ Module in

any combination. The connector pins are each rated for a maximum current of 500 mA.

ModSelL Pin

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP modules on a single 2-wire interface bus. When the ModSelL is "High", the module will not respond to any 2-wire interface communication from the host. ModSelL has an internal pull-up in the module.

ResetL Pin

Reset. LPMode_Reset has an internal pull-up in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the xecution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module will post this completion of reset interrupt without requiring a reset.

LPMode Pin

This Pin operate in the low power mode (less than 1.5 W power consumption).

ModPrsL Pin

ModPrsL is pulled up to Vcc on the host board and grounded in the module. The ModPrsL is asserted "Low" when the module is inserted and de-asserted "High" when the module is physically absent from the host connector.

IntL Pin

IntL is an output pin. When "Low", it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt by using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled up to Vcc on the host board.

Recommended Power Supply Filter

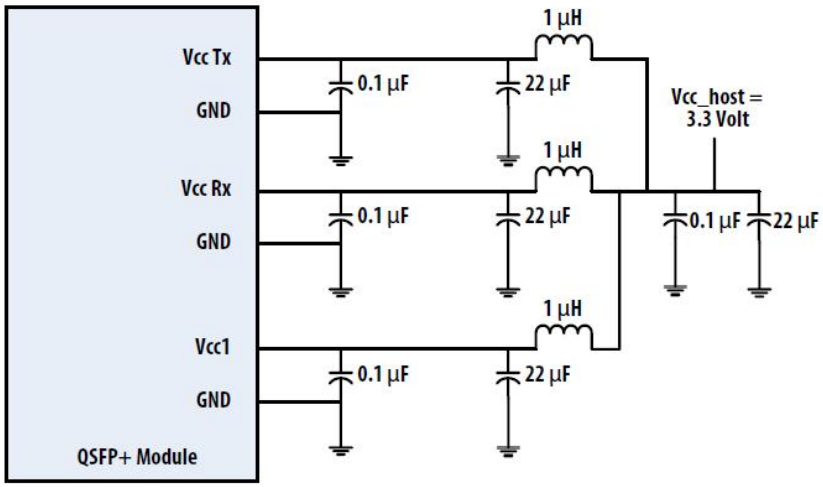

Figure 2 Recommended Power Supply Filter

Transceiver Block Diagram

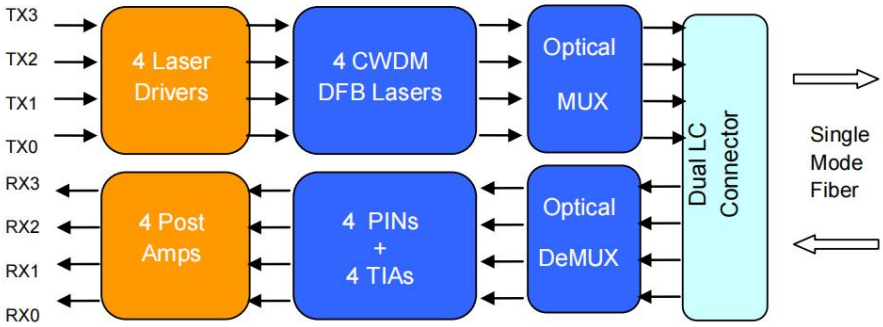

Figure 3 Transceiver Block Diagram

Mechanical Dimensions

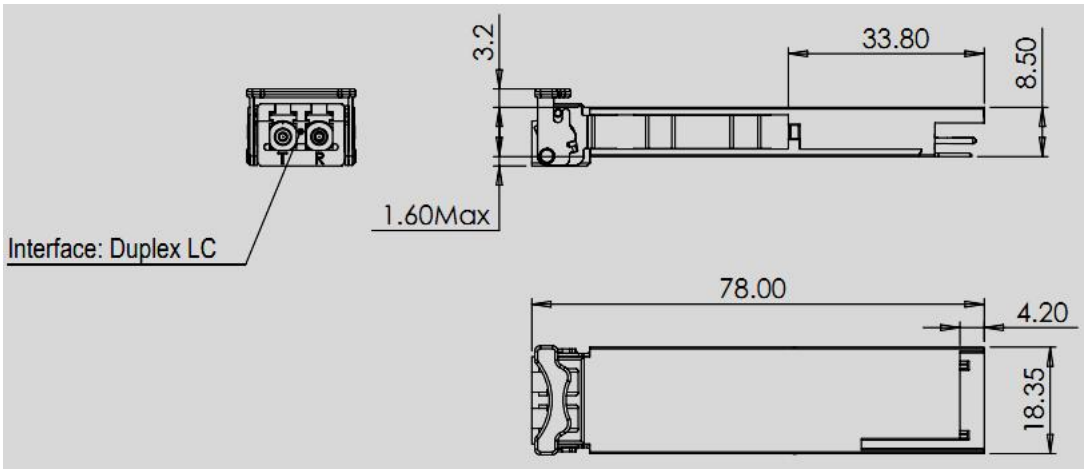

Figure 4 Mechanical Outline

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3. NADDOD assumes no responsibility for the use or reliability of equipment or software not provided by NADDOD.