100Gb/s QSFP28 ZR4 1310nm 80km Optical Transceiver

Features

- Compliant with 100GBASE-ZR4
- Support line rates from 103.125 Gb/s to 111.81 Gb/s OTU4
- LAN WDM EML laser and PIN receiver with SOA
- Up to 80km reach for G.652 SMF
- Hot pluggable 38 pin electrical interface
- QSFP28 MSA compliant
- Duplex LC optical receptacle
- Maximum power consumption 6.5W
- Case operating temperature: 0~70°C

Applications

- 100GBASE-ZR4 Ethernet Links
- Telecom networking

Compliance

- Compliant with SFF-8665
- Compliant with IEEE 802.3bm
- Compliant with OIF-CEI-04.0
- GR-468-CORE
- RoHS compliance

Description

The QSFP-100G-ZR4 Transceiver is designed for 80km optical communication applications. This module contains 4-lane optical transmitter, 4-lane optical receiver and module management block including 2 wire serial inter- face. The optical signals are multiplexed to a single-mode fiber through an industry standard LC connector.

Absolute Maximum Ratings

Table1-Absolute Maximum Ratings

Parameter	Symbols	Min.	Typical	Max.	Unit	Notes
Storage Temperature	TSTG	-40		+85	°C	
Operating Relative Humidity (non-condensing)	RH	15		85	%	
Power Supply Voltage	VCC	-0.5		4	V	
Damage Threshold,each Lane	THd	6.5			dBm	

Recommended Operating Conditions

Table2-Recommended Operating Conditions

Parameter	Symbols	Min.	Typical	Max.	Unit	Notes
Operating Case Temperature	Top	0		+70	°C	
Power Supply Voltage	VCC	3.315	3.3	3.465	V	
Data Rate,each Lane			25.78125		Gb/s	
Control Input Voltage High		2		Vcc	V	
Control Input Voltage Low		0		0.8	V	
Link Distance(SMF)	D			80	km	1

Notes:

[1] Depending on actual fiber loss/km (link distance specified is for fiber insertion loss of 0.35dB/km)

Electrical Characteristic

Table3-Electrical Characteristic

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Power Consumption	P			6.5	W	
Supply Current	Icc			1876	mA	

Optical Transmitter Characteristics						
Overload Differential Voltage pk-pk	TP1a			900	mV	
Common Mode Voltage (Vcm)	TP1	-350		2850	mV	1
Differential Termination Resistance Mismatch	TP1			10	%	At 1MHz
Differential Return Loss (SDD11)	TP1			See CEI-28G-VSR Equation 13-19	dB	
Common Mode to Differential conversion and Differential to Common Mode conversion (SDC11, SCD11)	TP1			See CEI-28G-VSR Equation 13-20	dB	
Stressed Input Test	TP1a	See CEI-28G-VSR Section 13.3.11.2.1				
Optical Receiver Characteristics						
Differential Voltage, pk-pk	TP4			900	mV	
Common Mode Voltage (Vcm)	TP4	-350		2850	mV	1
Common Mode Noise, RMS	TP4			17.5	mV	
Differential Return Loss (SDD22)	TP4			See CEI-28G-VSR Equation 13-19	dB	
Common Mode to Differential conversion and Differential to Common Mode conversion (SDC22, SCD22)	TP4			See CEI-28G-VSR Equation 13-21	dB	
Common Mode Return Loss (SCC22)	TP4			-2	dB	2
Transition Time, 20 to 80%	TP4	9.5			ps	
Vertical Eye Closure (VEC)	TP4			5.5	dB	
Eye Width at 10-15 probability (EW15)	TP4	0.57			UI	
Eye Height at 10-15 probability (EH15)	TP4	228			mV	

Notes:

[1] Vcm is generated by the host. Specification includes effects of ground offset voltage.

[2] From 250MHz to 30GHz.

Optical Characteristics

Table4-Optical Characteristics

Parameter	Symbols	Min.	Typical	Max.	Unit	Notes
Center Wavelength	L1	1294.53	1295.56	1296.59	nm	
	L2	1299.02	1300.05	1301.09	nm	
	L3	1303.54	1304.58	1305.63	nm	
	L4	1308.09	1309.14	1310.19	nm	
Transmitter						
Side-mode suppression ratio	SMSR	30			dB	
Total Launch Power	PT	8.0		12.5	dBm	
Average Launch Power,each Lane	PAVG	2.0		4.5	dBm	1
OMA,each Lane	POMA	0.1		4.5	dBm	2
Difference in Launch Power between any Two Lanes(OMA)	Ptx,diff			3.6	dB	
Launch Power in OMA minus Transmitter and Dispersion Penalty(TDP),each Lane	OMA-TDP	-0.65			dBm	
TDP,each Lane	TDP			2.5	dB	
Extinction Radio	ER	6.0			dB	
RIN20OMA	RIN			-130	dB/Hz	
Optical Return Loss Tolerance	TOL			20		
Transmitter Reflectance	RT			-12	dB	
Average Launch Power OFF Transmitter,each Lane	Poff			-30		
Eye Mask{X1,X2,X3,Y1,Y2,Y3}		{0.25,0.4,0.45,0.25,0.28,0.4}				
Receiver						
Average Receive Power, each Lane		-28		-3.5	dBm	
Receive Power (OMA), each Lane				-3.5	dBm	
Receiver reflectance	SEN1			-26	dBm	for BER = 1x10-12
Receiver sensitivity Average, each lane	SEN2			-28	dBm	for BER = 5x10-5

Difference in Receive Power between any Two Lanes (Average and OMA)	Ptx,diff			3.6	dB	
LOS Assert	LOSA	-40			dBm	
LOS Deassert	LOSD			-29	dBm	
LOS Hysteresis	LOSH	0.5			dB	
Conditions of Stress Receiver Sensitivity Test						
Vertical Eye Closure Penalty,each Lane			1.5		dB	
Stressed Eye J2 Jitter,each Lane			0.3		UI	
Stressed Eye J9 Jitter,each Lane			0.47		UI	

Notes:

[1] The minimum average launch power spec is based on ER not exceeding 9.5dB and transmitter OMA higher than 0.1dBm.

[2] Even if the TDP ＜ 0.75 dB, the OMA min must exceed the minimum value specified here.

Digital Diagnostic Functions

Table5-Digital Diagnostic Functions

Parameter	Symbols	Min.	Max.	Unit	Notes
Temperature monitor absolute error	DMI_Temp	-3	+3	degC	Over operating temperature range
Supply voltage monitor absolute error	DMI_VCC	-0.15	0.15	V	Over full operating range
Channel RX power monitor absolute error	DMI_RX_Ch	-3	+3	dB	
Channel Bias current monitor	DMI_Ibias_ Ch	-10%	10%	mA	
Channel TX power monitor absolute error	DMI_TX_Ch	-3	3	dB	

Pin Description

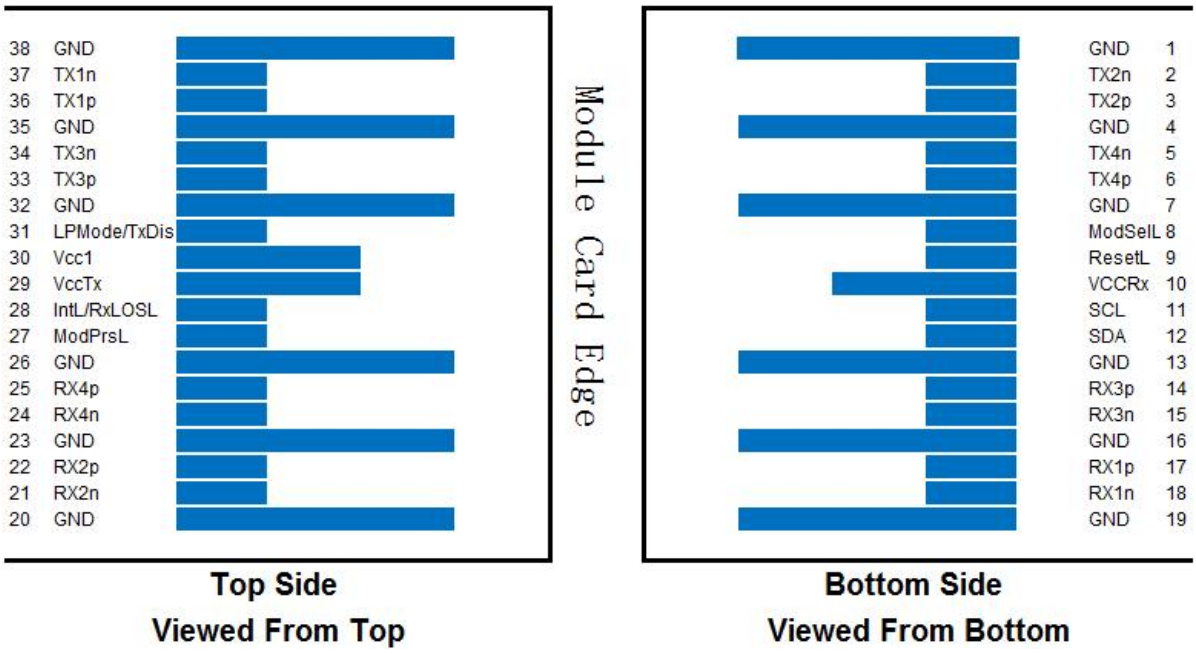

Figure 1 Pin view

Pin Function Definitions

Table6-Pin Function Definitions

Pin	Symbols	Description	Notes
1	GND	Ground	1
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data Input	
4	GND	Ground	1
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data Input	
7	GND	Ground	
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	Vcc Rx	+3.3V Power Supply Receiver	2
11	SCL	2-wire serial interface clock	
12	SDA	2-wire serial interface data	
13	GND	Ground	
14	Rx3p	Receiver Non-Inverted Data Output	

15	Rx3n	Receiver Inverted Data Output	
16	GND	Ground	1
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	1
19	GND	Ground	1
20	GND	Ground	
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Ground	
24	Rx4n	Receiver Inverted Data Output	
25	Rx4p	Receiver Non-Inverted Data Output	
26	GND	Ground	1
27	ModPrsL	Module Present	
28	IntL	Interrupt	
29	VccTx	+3.3V Power supply transmitter	2
30	Vcc1	+3.3V Power supply	2
31	LPMode	Low Power Mode	
32	GND	Ground	1
33	Tx3p	Transmitter Non-Inverted Data Input	
34	Tx3n	Transmitter Inverted Data Input	
35	GND	Ground	1
36	Tx1p	Transmitter Non-Inverted Data Input	
37	Tx1n	Transmitter Inverted Data Input	
38	GND	Ground	1

Notes:

[1] GND is the symbol for signal and supply (power) common for the module. All are common within the module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

[2] Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Recommended host board power supply filtering is shown in Figure2. Vcc Rx Vcc1 and Vcc Tx may be internally connected within the Module in any combination. The connector pins are each rated for a maximum current of 1000 mA.

ModSelL

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple modules on a single 2-wire interface bus. When the ModSelL is "High", the module shall not respond to or acknowledge any 2-wire interface communication from the host. ModSelL signal input node shall be biased to the "High" state in the module.

In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any modules are deselected. Similarly, the host shall wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.

Transceiver Block Diagram

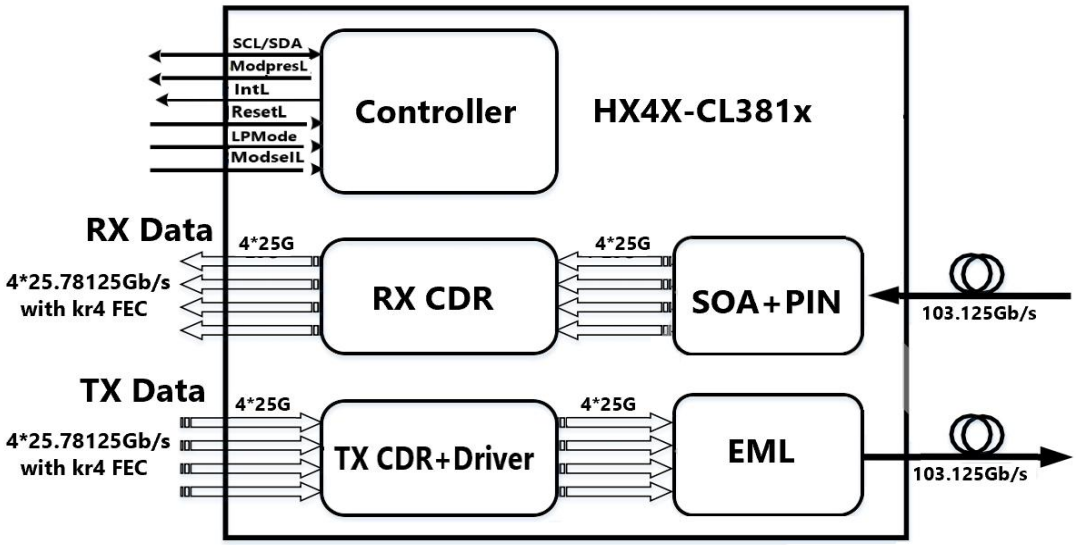

Figure 2 Transceiver Block Diagram

ResetL:

The ResetL pin shall be pulled to Vcc in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by asserting "low" an IntL signal with the Data Not_Ready bit negated. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

LPMode:

LPMode: The LPMode pin shall be pulled up to Vcc in the module. The pin is a hardware control used to put modules into a low power mode when high. By using the LPMode pin and a combination of the Power override, Power_set and High_Power_Class_Enable software control bits (Address A0h, byte 93 bits 0,1,2).

ModPrsL:

ModPrsL is pulled up to Vcc_Host on the host board and grounded in the module. The ModPrsL is asserted "Low" when inserted and deasserted "High" when the module is physically absent from the host connector.

IntL:

IntL is an output pin. When IntL is "Low", it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and shall be pulled to host supply voltage on the host board. The INTL pin is deasserted "High" after completion of reset, when byte 2 bit 0 (Data Not Ready) is read with a value of '0' and the flag field is read .

Mechanical Dimensions

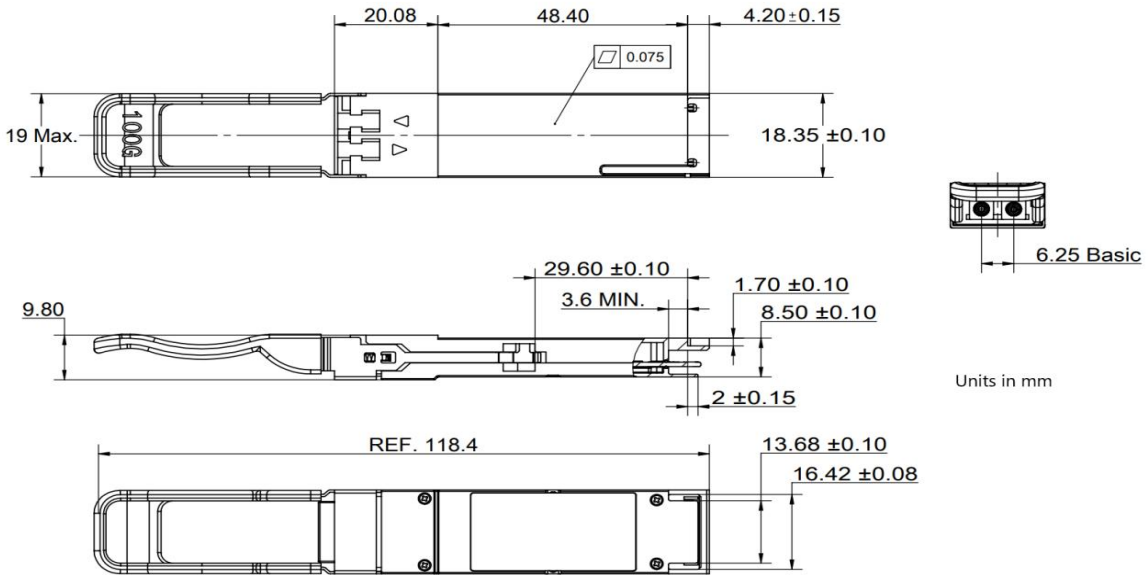

Figure 3 Mechanical Dimensions

ESD

This transceiver is specified as ESD threshold 1kV for high speed data pins and 2kV for all other electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

Laser Safety

This is a Class 1 Laser Product according to EN 60825-1:2014. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007).

Caution: Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

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3. NADDOD assumes no responsibility for the use or reliability of equipment or software not provided by NADDOD.