

800Gb/s OSFP DR8 1310nm 500m Optical Transceiver

Features

- Compliant with IEEE 802.3cu-2021: -2x400GBASE-DR4 optical interface
- Compliant with IEEE P802.3ck D2.2 -2x400GAUI-4 C2M electrical interface
- Compliant with OSFP MSA HW Rev 4.1 Type 2 housing with Dual MPO-12 connector
- Compliant with CMIS Rev 5.0
- Maximum Power Consumption 16w
- Operating Temperature Range: 0°C ~ +70 °C
- Two Wire Serial Interface with Digital Diagnostic Monitoring
- Class 1 Laser Safety

Applications

- 800G Ethernet
- 2x 400GBASE-DR4
- Data Center
- Cloud Networks

Description

The OSFP-800G-DR8 transceiver supports up to 500m link lengths over single-mode fiber (SMF) via dual MTP/MPO-12 connectors. This transceiver is compliant with IEE802.3ck, IEEE 802.3cu and OSFP MSA standards. The built-in digital diagnostics monitoring (DDM) allows access to real-time operating parameters. It is suitable for 800G Ethernet, Breakout 2x 400G DR4, Data Center and Cloud Networks.

Absolute Maximum Ratings

Table1-Absolute Maximum Ratings						
Parameter	Symbols	Min.	Typical	Max.	Unit	Notes
Storage Temperature	TS	-40		+85	°C	
Operating Relative Humidity (non-condensing)	R _H	5		95	%	
Supply Voltage	V _{CC}	-0.5		3.6	V	
Data Input Voltage Differential	I _{VDIP} -V _{DIN}			1	V	
Control Input Voltage	V _I	-0.3		V _{CC} +0.5	V	
Control Output Current	I _O	-20		20	mA	

Recommended Operating Conditions

Table2-Recommended Operating Conditions						
Parameter	Symbols	Min.	Typical	Max.	Unit	Notes
Operating Case Temperature	T _{op}	0		+70	°C	
Power Supply Voltage	V _{CC}	3.135	3.3	3.465	V	
Instantaneous peak current at hot plug	I _{CC_IP}				mA	
Sustained peak current at hot plug	I _{CC_SP}				mA	
Maximum Power Dissipation	P _D			16	W	
Maximum Power Dissipation, Low Power Mode						
Control Input Voltage High	V _{IH}	V _{CC} *0.7		V _{CC} +0.3	V	
Control Input Voltage High	V _{IH}	V _{CC} *0.7		V _{CC} +0.3	V	
Control Input Voltage Low	V _{IL}	-0.3		V _{CC} *0.3	V	
Two Wire Serial Interface Clock Rate				400	kHz	
Power Supply Noise 1 kHz - 1 MHz (p-p)				66	mVpp	
Operating Distance		2		500	m	

Electrical Characteristic

Table3-Electrical Characteristic

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Transmitter						
AC common-mode output Voltage (RMS)				25	mV	
Differential peak-to-peak output voltage				600	mV	
Short mode				900	mV	
Long mode						
Eye height, differential	EH	15			mV	
Vertical eye closure	VEC			12	dB	
Common-mode to differential return loss	RLDc	802.3ck 120G- 1			dB	
Effective return loss, ERL	ERL	8.5			dB	
Differential termination mismatch				10	%	
Transition time (20% to 80%)		8.5			ps	
Receiver						
Differential pk-pk input Voltage tolerance		900			mV	
AC common-mode RMSvoltage tolerance (TP1a)		25			mV	
Differential to common-mode return loss	RLcd	802.3ck 120G-2			dB	
Effective return loss, ERL	ERL	8.5			dB	
Differential termination mismatch				10	%	
Single-ended voltage tolerance range		-0.4		3.3	V	
DC common-mode Voltage		-0.35		2.85	V	

Optical Characteristics

Table4-Optical Characteristics

Parameter	Symbols	Min.	Typical	Max.	Unit	Notes
Wavelength	λ_c	1304.5	1311	1317.5	nm	
Transmitter						
Side Mode Suppression Ratio	SMSR	30			dB	
Average Launch Power, each lane	AOPL	-2.9		4.0	dBm	1
Outer Optical Modulation Amplitude (OMA _{outer}), each Lane	TOMA	-0.8		4.2	dBm	
Launch Power in OMA _{outer} minus TDECQ, each lane	TOMA-TDECQ	-2.2			dBm	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each lane	TDECQ			3.4	dB	
Average Launch Power of OFF Transmitter, each lane	TOFF			- 15	dBm	
Extinction Ratio	ER	3.5			dB	
Transmitter transition time (max)	Tr			17	ps	
RIN21.4OMA (max)	RIN			- 136	dB/Hz	
Optical Return Loss Tolerance	ORL			21.4	dB	
Transmitter Reflectance	TR			-26	dB	2
Receiver						
Wavelength L0	λ_{C0}	1304.5	1311	1317.5	nm	
Damage Threshold, each Lane	AOPD	5			dBm	
Average Receive Power, each Lane	AOPR	-5.9		4	dBm	
Receive Power (OMA _{outer}), each Lane	OMAR			4.2	dBm	
Receiver Reflectance	RR			-26	dB	
Receiver Sensitivity (OMA _{outer}), each Lane	SOMA			Max[-3.9, SECQ - 5.3]	dBm	3
Stressed Receiver Sensitivity (OMA _{outer}), each Lane	SRS			- 1.9	dBm	4
LOS De-assert	LOSD			-12	dBm	
LOS Hysteresis	LOSH	0.5			dB	
Conditions of stressed receiver sensitivity test						

Stressed eye closure for PAM4(SECQ), lane under test	SECQ		3.4		dB	
OMA _{outer} of each aggressor lane			4.2			

Notes:

- [1] Average launch power, each lane (min) is informative and not the principal indicator of signal strength
- [2] Transmitter reflectance is defined looking into the transmitter
- [3] Receiver sensitivity (OMA_{outer}), each lane (max) is informative and is defined for a transmitter with a value of SECQ up to 3.4 dB.
- [4] Measured with conformance test signal at TP3 for the BER = 2.4x10⁻⁴

Electrical Specification Low Speed Signal

Parameter	Symbols	Min.	Max.	Unit	Notes
Module output SCL and SDA	VOL	0	0.4	V	
Module Input SCL and SDA	VIL	-0.3	VCC*0.3	V	
	VIH	VCC*0.7	VCC+0.5	V	
LPMode/TxDis, ResetL and ModSelL	VIL	-0.3	0.8	V	
	VIH	2	VCC+0.3	V	
IntL/RxLos	VOL	0	0.4	V	
	VOH	VCC-0.5	VCC+0.3	V	

Pin Description

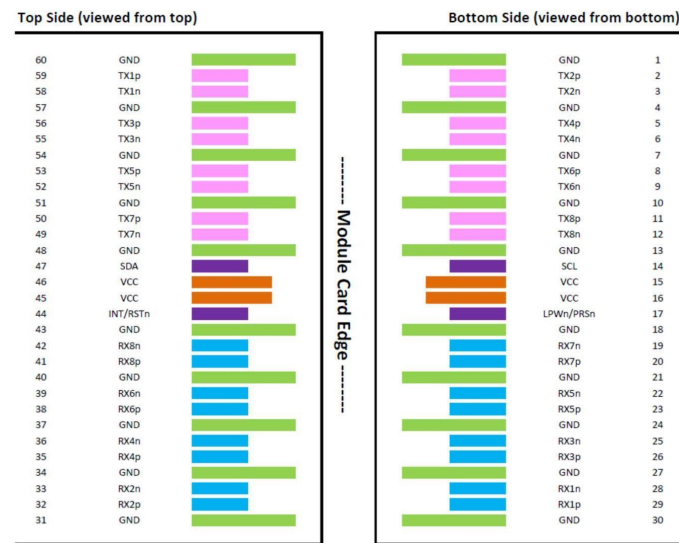


Figure 1 Pinout definitions of OSFP module inputs/outputs

Pin Function Definitions

Table6-Pin Function Definitions

Pin	Symbol	Description	Logic	Notes
1	GND	Ground		
2	TX2p	Transmitter Data Non-Inverted	CML-I	
3	TX2n	Transmitter Data Inverted	CML-I	
4	GND	Ground		
5	TX4p	Transmitter Data Non-Inverted	CML-I	
6	TX4n	Transmitter Data Inverted	CML-I	
7	GND	Ground		
8	TX6p	Transmitter Data Non-Inverted	CML-I	
9	TX6n	Transmitter Data Inverted	CML-I	
10	GND	Ground		
11	TX8p	Transmitter Data Non-Inverted	CML-I	
12	TX8n	Transmitter Data Inverted	CML-I	
13	GND	Ground		
14	SCL	2-wire Serial interface clock	LVCMOS-I/O	
15	VCC	+3.3V Power		
16	VCC	+3.3V Power		
17	LPWn/P RSn	Low-Power Mode / Module Present	Multi-Level	
18	GND	Ground		
19	RX7n	Receiver Data Inverted	CML-O	
20	RX7p	Receiver Data Non-Inverted	CML-O	
21	GND	Ground		

22	RX5n	Receiver Data Inverted	CML-O	
23	RX5p	Receiver Data Non-Inverted	CML-O	
24	GND	Ground		
25	RX3n	Receiver Data Inverted	CML-O	

Recommended OSFP Host Board Schematic

27	GND	Ground		
28	RX1n	Receiver Data Inverted	CML-O	
29	RX1p	Receiver Data Non-Inverted	CML-O	
30	GND	Ground		
31	GND	Ground		
32	RX2p	Receiver Data Non-Inverted	CML-O	
33	RX2n	Receiver Data Inverted	CML-O	
34	GND	Ground		
35	RX4p	Receiver Data Non-Inverted	CML-O	
36	RX4n	Receiver Data Inverted	CML-O	
37	GND	Ground		
38	RX6p	Receiver Data Non-Inverted	CML-O	
39	RX6n	Receiver Data Inverted	CML-O	
40	GND	Ground		
41	RX8p	Receiver Data Non-Inverted	CML-O	
42	RX8n	Receiver Data Inverted	CML-O	
43	GND	Ground		
44	INT/RSTn	Module Interrupt / Module Reset	Multi- Level	
45	VCC	+3.3V Power		
46	VCC	+3.3V Power		
47	SDA	2-wire Serial interface data	LVCM OS-I/O	
48	GND	Ground		
49	TX7n	Transmitter Data Inverted	CML-I	
50	TX7p	Transmitter Data Non-Inverted	CML-I	
51	GND	Ground		
52	TX5n	Transmitter Data Inverted	CML-I	
53	TX5p	Transmitter Data Non-Inverted	CML-I	
54	GND	Ground		
55	TX3n	Transmitter Data Inverted	CML-I	
56	TX3p	Transmitter Data Non-Inverted	CML-I	
57	GND	Ground		
58	TX1n	Transmitter Data Inverted	CML-I	
59	TX1p	Transmitter Data Non-Inverted	CML-I	
60	GND	Ground		

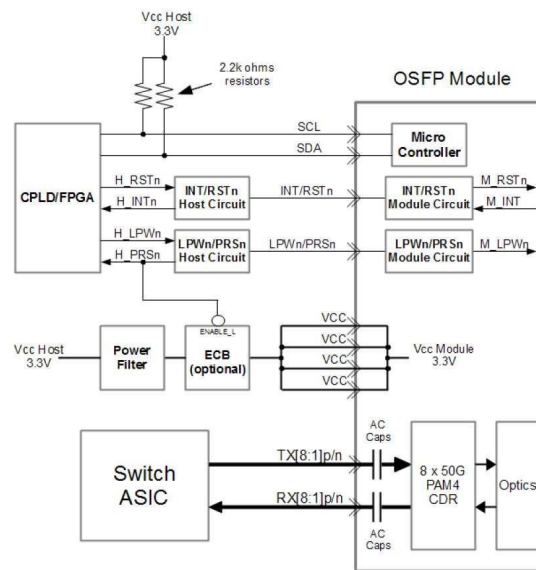


Figure 2 Recommended OSFP Host Board Schematic

Digital Diagnostics

Parameter	Range	Accuracy	Unit	Calibration
Temperature	0 to 70	±3	°C	Internal
Voltage	0 to VCC	0.1	V	Internal
Tx Bias Current (Each Lane)	0 to 100	10%	mA	Internal
Tx Output Power (Each Lane)	-2.8 to +5.3	±3	dB	Internal
Rx Receive Power (Each Lane)	-9.1 to +5.3	±3	dB	Internal

Mechanical Dimensions

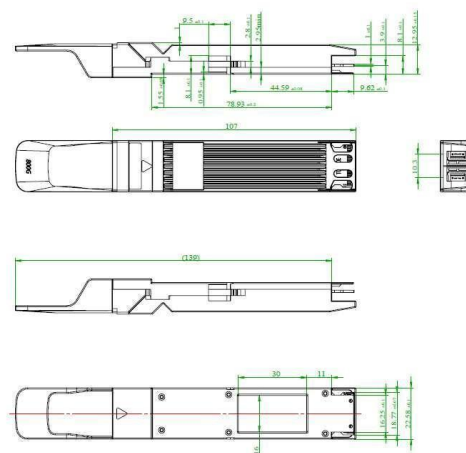


Figure 3 Mechanical Outline

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