

800Gb/s DR8+ OSFP 1310nm 2km MTP/MPO-16 Optical Transceiver

Features

- Compliant with IEEE 802.3cu-2021: 8x100GBASE-FR1 Optical Interface
- Compliant with IEEE P802.3ck D3.0: 8x100GAUI-1 C2M Electrical Interface
- Compliant with OSFP MSA HW Rev 4.1 Type 2 Housing with MPO-16 Connector
- Compliant with CMIS Rev 5.0
- Case Operating Temperature: 0°C to 70°C
- Two Wire Serial Interface with Digital Diagnostic Monitoring
- Complies with EU Directive 2011/65/EU
- Class 1 Laser

Applications

- 800G Ethernet
- Data Center

Description

The 800GBASE-XDR8 OSFP Optical Transceiver Module is designed for 800GBASE Ethernet throughput up to 2 km over single mode fiber (SMF) with MPO-16 connectors. This transceiver is compliant with IEEE802.3ck, IEEE 802.3cu, OSFP MSA. The built-in digital diagnostics monitoring (DDM) allows access to real-time operating parameters. It is suitable for 800G Ethernet, Data Center, Breakout 2x 400G XDR4 or 8x 100G FR Application.

Absolute Maximum Ratings

Table1-Absolute Maximum Ratings

Parameter	Symbols	Min.	Max	Unit	Notes
Storage Temperature Range	TS	-40	85	°C	
Supply Voltage	VCC	-0.5	3.6	V	
Relative Humidity (non-condensing)	RH	5	95	%	
Data Input Voltage Differential	IVDIP-VDINL		1	V	
Control Input Voltage	VI	-0.3	VCC+0.5	V	
Control Output Current	IO	-20	20	mA	

Recommended Operating Conditions

Table2-Recommended Operating Conditions

Parameter	Symbols	Min.	Typical	Max.	Unit	Notes
Operating Case Temperature	TOPR	0		70	°C	1
Power Supply Voltage	VCC	3.135	3.3	3.465	V	
Instantaneous peak current at hot plug	ICC_IP			TBD	mA	
Sustained peak current at hot plug	ICC_SP			TBD	mA	
Maximum Power Dissipation	PD			TBD	W	
Maximum Power Dissipation, Low Power Mode	PDLP			2	W	
Signaling Speed per Lane	DRL		53.125		GBd	
Control Input Voltage High	VIH	VCC*0.7		VCC+0.3	V	
Control Input Voltage Low	VIL	-0.3		VCC*0.3	V	
Two Wire Serial Interface Clock Rate				400	kHz	
Power Supply Noise 1 kHz - 1 MHz (p-p)				66	mVpp	
Operating Distance		2		2000	m	

Optical Characteristic

Table3-Optical Characteristic						
Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Transmitter						
Wavelength	λ_C	1304.5	1311	1317.5	nm	
Side Mode Suppression Ratio	SMSR	30			dB	
Average Launch Power, each Lane	AOPL	-3.1		4.0	dBm	1
Outer Optical Modulation Amplitude (OMA _{outer}), each Lane for TDECQ < 1.4dB for 1.4dB ≤ TDECQ ≤ 3.4dB	OMA _{outer}	-0.1 - 1.5 +TDECQ		4.2	dBm	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each Lane	TDECQ			3.4	dB	
Transmitter Eye Closure for PAM4 (TECQ), each Lane	TECQ			3.4	dB	
TDECQ-TECQ				2.5	dB	
Over/Under-shoot				22	%	
Transmitter Power Excursion				2	dBm	
Average Launch Power of OFF Transmitter, each Lane	TOFF			- 15	dBm	
Extinction Ratio	ER	3.5			dB	
Transmitter Transition Time	Tr			17	ps	
RIN17. 10MA	RIN			- 136	dB/Hz	
Optical Return Loss Tolerance	ORL			17.1	dB	
Transmitter Reflectance	TR			-26	dB	2
Receiver						
Wavelength	λ_{C0}	1304.5	1311	1317.5	nm	
Damage Threshold, each Lane	AOPD	5			dBm	
Average Receive Power, each Lane	AOPR	-7.1		4	dBm	
Receive Power (OMA _{outer}),each Lane	OMAR			4.2	dBm	
Receiver Reflectance	RR			-26	dB	
Receiver Sensitivity (OMA _{outer})for TECQ < 1.4 dB for 1.4dB ≤ TECQ ≤ 3.4dB	SOMA			-4.5- 5.9+TECQ	dBm	3
Stressed Receiver Sensitivity (OMA _{outer}), each Lane	SRS			-2.5	dBm	4
Conditions of stressed receiver sensitivity test:						
Stressed eye closure for PAM4 (SECQ), lane under test			3.4		dB	

Notes:

1.Average launch power, each lane [min] is informative and not the principal indicator of signal strength 2. Transmitter reflectance is

defined looking into the transmitter.

3. Receiver sensitivity (OMA_{outer}), each lane (max) is informative and is defined for a transmitter with a value of SECQ up to 3.4 dB.

4. Measured with conformance test signal at TP3 for the BER = 2.4×10^{-4}

Electrical Specification High Speed Signal (compliant with IEEE P802.3ck C2M))

Table4-Electrical Characteristics

Parameter	Symbols	Min.	Typical	Max.	Unit	Notes
Receiver (Module Output, TP4)						
AC common-mode output Voltage (RMS)				25	mV	
Differential peak-to-peak Output Voltage				600	mV	
Short Mode Long Mode				845	mV	
Eye Height	EH	15			mV	
Vertical Eye Closure	VEC			12	dB	
Common-mode to Differential-mode Return Loss	RLDc	802.3ck120G- 1			dB	
Effective Return Loss	ERL	8.5			dB	
Differential Termination Mismatch				10	%	
Transition Time		8.5			ps	
DC Common-mode Voltage Tolerance		-0.35		2.85	V	
Transmitter (Module Input, TP1)						
Differential pk-pk Input Voltage Tolerance(TP1a)		750			mV	
AC Common-mode RMS Voltage Tolerance(TP1a)		25			mV	
Differential-mode to Common-mode Return Loss	RLcd	802.3ck120G-2			dB	
Effective Return Loss	ERL	8.5			dB	
Differential Termination Mismatch				10	%	
Single-ended Voltage Tolerance Range		-0.4		3.3	V	
DC Common-mode Voltage Tolerance		-0.35		2.85	V	

Electrical Specification Low Speed Control and Sense Signals (compliant with QSFP-DD HW Rev 6.01)

Table5-Electrical Characteristics

Parameter	Symbols	Min.	Max	Unit	Notes
Module Output SC Land SDA	VOL	0	0.4	V	
Module Input SCL and SDA	VIL	-0.3	VCC*0.3	V	
	VIH	VCC*0.7	VCC+0.5	V	
InitMode, ResetL and ModSelL	VIL	-0.3	0.8	V	
	VIH	2	VCC+0.3	V	
IntL	VOL	0	0.4	V	
	VOH	VCC-0.5	VCC+0.3	V	

Pin Description

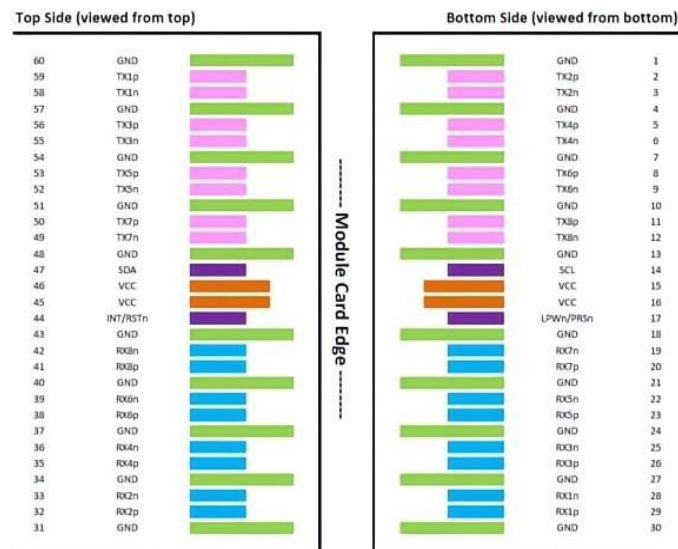


Figure 1 Pinout definitions of OSFP module inputs/outputs

Pin Function Definitions

Table5-Pin Function Definitions				
Pin	Symbol	Description	Logic	Notes
1	GND	Ground		
2	TX2p	Transmitter Data Non-Inverted	CML-I	
3	TX2n	Transmitter Data Inverted	CML-I	
4	GND	Ground		
5	TX4p	Transmitter Data Non-Inverted	CML-I	
6	TX4n	Transmitter Data Inverted	CML-I	
7	GND	Ground		
8	TX6p	Transmitter Data Non-Inverted	CML-I	
9	TX6n	Transmitter Data Inverted	CML-I	
10	GND	Ground		
11	TX8p	Transmitter Data Non-Inverted	CML-I	
12	TX8n	Transmitter Data Inverted	CML-I	
13	GND	Ground		
14	SCL	2-wire Serial interface clock	LVC MOS-I/O	
15	VCC	+3.3V Power		
16	VCC	+3.3V Power		
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	
18	GND	Ground		
19	RX7n	Receiver Data Inverted	CML-O	

20	RX7p	Receiver Data Non-Inverted	CML-0	
21	GND	Ground		
22	RX5n	Receiver Data Inverted	CML-0	
23	RX5p	Receiver Data Non-Inverted	CML-0	
24	GND	Ground		
25	RX3n	Receiver Data Inverted	CML-0	
26	RX3p	Receiver Data Non-Inverted	CML-0	
27	GND	Ground		
28	RX1n	Receiver Data Inverted	CML-0	
29	RX1p	Receiver Data Non-Inverted	CML-0	
30	GND	Ground		
31	GND	Ground		
32	RX2p	Receiver Data Non-Inverted	CML-0	
33	RX2n	Receiver Data Inverted	CML-0	
34	GND	Ground		
35	RX4p	Receiver Data Non-Inverted	CML-0	
36	RX4n	Receiver Data Inverted	CML-0	
37	GND	Ground		
38	RX6p	Receiver Data Non-Inverted	CML-0	
39	RX6n	Receiver Data Inverted	CML-0	
40	GND	Ground		
41	RX8p	Receiver Data Non-Inverted	CML-0	
42	RX8n	Receiver Data Inverted	CML-0	
43	GND	Ground		
44	INT/RSTn	Module Interrupt / Module Reset	Multi- Level	
45	VCC	+3.3V Power		
46	VCC	+3.3V Power		
47	SDA	2-wire Serial interface data	LVCM OS-I/O	
48	GND	Ground		
49	TX7n	Transmitter Data Inverted	CML-I	
50	TX7p	Transmitter Data Non-Inverted	CML-I	
51	GND	Ground		
52	TX5n	Transmitter Data Inverted	CML-I	
53	TX5p	Transmitter Data Non-Inverted	CML-I	
54	GND	Ground		
55	TX3n	Transmitter Data Inverted	CML-I	
56	TX3p	Transmitter Data Non-Inverted	CML-I	
57	GND	Ground		
58	TX1n	Transmitter Data Inverted	CML-I	
59	TX1p	Transmitter Data Non-Inverted	CML-I	
60	GND	Ground		

Recommended OSFP Host Board Schematic

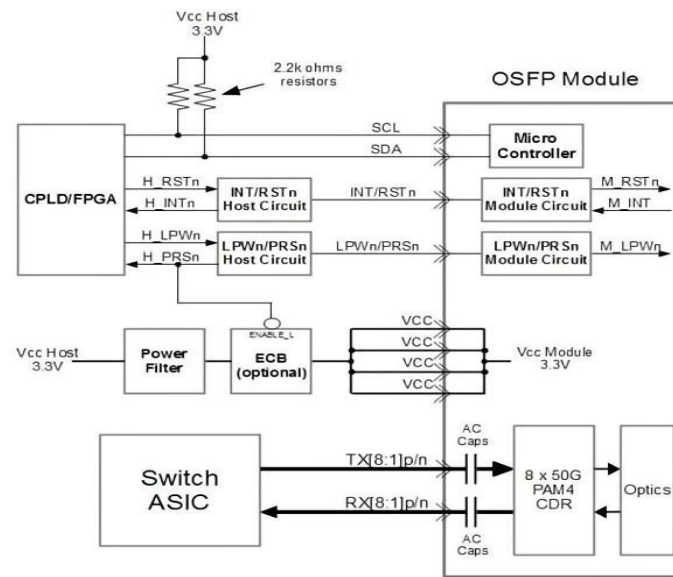
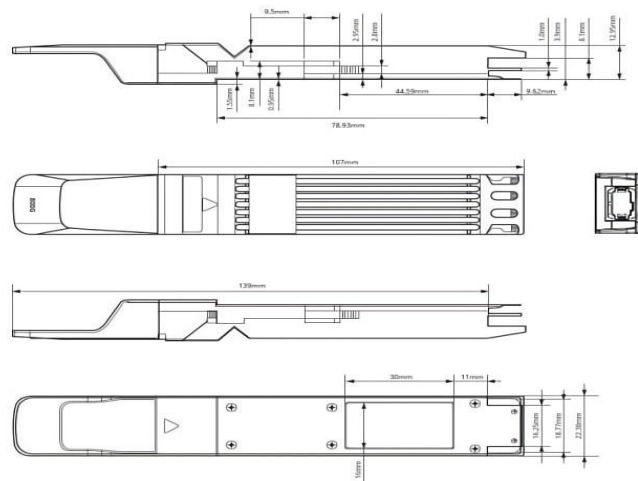


Figure 2 Recommended OSFP Host Board Schematic

Digital Diagnostics

Parameter	Range	Accuracy.	Unit	Calibration
Temperature	0~70	±3	°C	Internal
Voltage	0~VCC	0.1	V	Internal
Tx Bias Current (each Lane)	0~100	10%	mA	Internal
Tx Output Power (each Lane)	-3.1~4	±3	dB	Internal
Rx Receive Power (each Lane)	-7.1~4	±3	dB	Internal

Mechanical Diagram



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