

# 800Gb/s OSFP SR8 850nm 50m Optical Transceiver

## Features

- 53.125 GBd PAM4 ×8 channel 800G-SR8 Optical interface
- 53.125 GBd PAM4 ×8 channel 800G AUI-8 C2M Electrical interface
- Up to 50m transmission distance on OM4 MMF
- 850nm VCSEL and PIN receiver
- OSFP MSA package with MPO-16 APC
- +3.3V power supply
- Power consumption less than 12W
- Operating case temperature: 0~70°C
- IIC rate up to 1MHz

## Applications

- 800G Ethernet
- Data Center
- Cloud Networks

## Compliance

- OSFP MSA
- IEEE 802.3ck
- CMIS Rev4.0
- RoHS compliance

## Description

The OSFP-800G-SR8 transceiver is a cost effective module with high performance, which is optimized for Data Center, supporting data-rate of 8x53.125 GBd PAM4. Its transmission distance is up to 50m on OM4 MMF. The module mainly consists of two parts: the transmitter part and the receiver part. The transmitter part consists of an 850nm VCSEL array and a driver. The receiver part consists of a trans-impedance amplifier (TIA) and a PIN photodiode array. The high-speed electrical interface is based on low-voltage logic, with nominal 100 ohm differential impedance, AC coupled in the module. Users can access a series of registers in transceiver to access monitoring and configuration data through two wire serial interface.

## Absolute Maximum Ratings

**Table1-Absolute Maximum Ratings**

| Parameter                                    | Symbols         | Min. | Typical | Max. | Unit | Notes |
|--|-----------------|------|---------|------|------|-------|
| Storage Temperature                          | TS              | -40  |         | +85  | °C   |       |
| Operating Relative Humidity (non-condensing) | R <sub>H</sub>  | 5    |         | 85   | %    |       |
| Supply Voltage                               | V <sub>CC</sub> | 3.1  |         | 3.6  | V    |       |
| Optical Input Power                          | PIN             |      |         | 10   | dBm  |       |

## Recommended Operating Conditions

**Table2-Recommended Operating Conditions**

| Parameter                  | Symbols | Min.  | Typical | Max.  | Unit | Notes |
|----------------------------|---------|-------|---------|-------|------|-------|
| Operating Case Temperature | Top     | 0     |         | +70   | °C   |       |
| Power Supply Voltage       | VCC     | 3.135 | 3.3     | 3.465 | V    |       |
| Supply Current             | ICC     |       |         | 4000  | mA   |       |
| Module Power Dissipation   | P       |       |         | 12    | W    |       |

## Optical, Electrical Characteristic

**Table3-Transmitter Operating Characteristic-Optical, Electrical**

| Parameter                      | Symbols          | Min. | Typical | Max. | Unit | Notes |
|--------------------------------|------------------|------|---------|------|------|-------|
| Data Rate per channel (PAM4)   | DR               |      | 53.125  |      | GBd  |       |
| Frequency tracking             | Ft               | -100 |         | 100  | Ppm  |       |
| Center Wavelength              | $\lambda$ C      |      | 850     |      | nm   |       |
| RMS Spectral Width             |                  |      |         | 0.6  | nm   | Note1 |
| Laser Off Power                | P <sub>off</sub> |      |         | -30  | dBm  |       |
| Average Optical Power          | P <sub>avg</sub> | -4.6 |         | 4    | dBm  |       |
| Extinction Ratio               | ER               | 3.5  |         |      | dB   |       |
| Transmitter and dispersion eye | TDECQ            |      |         | 4.4  | dBm  |       |

|                                    |                      |      |   |     |    |       |
|------------------------------------|----------------------|------|---|-----|----|-------|
| closure                            |                      |      |   |     |    |       |
| Outer Optical Modulation Amplitude | OMA <sub>outer</sub> | -2.6 |   | 3.5 |    | Note2 |
| Encircled flux, each lane c        | dB                   |      | $\geq 86\% @ 19 \mu m$<br>$\leq 30\% @ 4.5 \mu m$ |     |    | Note3 |
| Optical Return Loss Tolerance      |                      |      |   | 12  | dB |       |

Notes:

- [1] RMS spectral width is the standard deviation of the spectrum.
- [2] Even if the TDECQ<51.8dB, the OMA (min) must exceed this value.
- [3] If measured into type A1a.2, type A1a.3 or type A1a.4, 50  $\mu m$  fiber, in accordance with IEC 61280-1-4.

## Receiver Operating Characteristic-Optical, Electrical

| Table4-Receiver Operating Characteristic-Optical, Electrical |                  |       |         |      |      |       |
|--|------------------|-------|---------|------|------|-------|
| Parameter  | Symbols          | Min.  | Typical | Max. | Unit | Notes |
| Data Rate per channel (PAM4)                                 | DR               |       | 53.125  |      | GBd  |       |
| Frequency tracking   | Ft               | -100  |         | 100  | Ppm  |       |
| Center Wavelength  | $\lambda_r$      | 840   | 850     | 860  | nm   |       |
| Damage threshold   |                  | 5     |         |      | dBm  |       |
| Average receive power  |                  | -4.6  |         | 4    | dBm  | Note1 |
| Receiver Reflectance   |                  |       |         | -15  | dB   |       |
| Differential Data Output Voltage Peak to Peak Swing          | V <sub>opp</sub> |       |         | 845  | mV   |       |
| Eye height   | EH               | 15    |         |      | mV   |       |
| Vertical eye closure   | VEC              |       |         | 12   | dB   |       |
| Differential output Impedance                                | Z <sub>os</sub>  | 90    | 100     | 110  | Ohms |       |
| Common-Mode to differential-mode return loss                 | RL <sub>dc</sub> | Note2 |         |      |      |       |
| Transition Time, 20 to 80%                                   | Tr, Tf           | 8.5   |         |      | ps   |       |

Notes:

- [1] Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
- Receiver sensitivity is informative and is defined for a transmitter with a value of SECQ up to 4.6 dB.

[2] 
$$RL_{dc}(f) \geq \begin{cases} 25 - 22(f/53.125) & 0.05 \leq f \leq 26.56 \\ 19 - 10(f/53.125) & 26.56 < f \leq 50 \end{cases}$$

## Digital Diagnostic Functions

**Table5-Digital Diagnostic Functions**

| Parameter                             | Symbols   | Min. | Max. | Unit | Notes |
|---------------------------------------|-----------|------|------|------|-------|
| Temperature monitor absolute error    | DMI_Temp  | -3   | 3    | °C   |       |
| Tx power monitor absolute error       | DMI_TX    | -3   | 3    | dB   |       |
| Rx power monitor absolute error       | DMI_RX    | -3   | 3    | dB   |       |
| Supply voltage monitor absolute error | DMI_VCC   | -3   | 3    | %    |       |
| Bias current monitor absolute error   | DMI_Ibias | -10  | 10   | %    |       |

## Control and Status I/O Timing Characteristics

**Table6-Control and Status I/O Timing Characteristics**

| Parameter          | Symbols                  | Min. | Typ | Max. | Unit | Notes |
|--------------------|--------------------------|------|-----|------|------|-------|
| Mgmt Init Duration | Max MgmtInit<br>Duration |      | TBD |      | ms   | Note1 |
| ResetL Assert Time | t_reset_init             |      | TBD |      | μs   | Note2 |
| IntL Assert Time   | ton_IntL                 |      | TBD |      | ms   | Note3 |
| IntL Deassert Time | toff_IntL                |      | TBD |      | μs   | Note4 |
| Rx LOS Assert Time | ton_los                  |      | TBD |      | ms   | Note5 |
| Flag Assert Time   | ton_flag                 |      | TBD |      | ms   | Note6 |
| Mask Assert Time   | ton_mask                 |      | TBD |      | ms   | Note7 |
| Mask Deassert Time | toff_mask                |      | TBD |      | ms   | Note8 |

Notes:

- [1] Time from power on, hot plug or rising edge of reset until completion of the MgmtInit State.
- [2] Minimum pulse time on the ResetL signal to initiate a module reset.
- [3] Time from occurrence of condition triggering IntL until Vout:IntL=Vol.
- [4] Time from clear on read operation of associated flag until Vout:IntL=Voh.This includes deassert times for Rx LOS, Tx Fault and other flag bits.
- [5] Time from Rx LOS state to Rx LOS bit set (value = 1b) and IntL asserted.
- [6] Time from occurrence of condition triggering flag to associated flag bit set (value=1b) and IntL asserted.
- [7] Time from mask bit set (value=1b) until associated IntL assertion is inhibited.
- [8] Time from mask bit cleared (value=0b) until associated IntL operation resumes.

## Pin Description

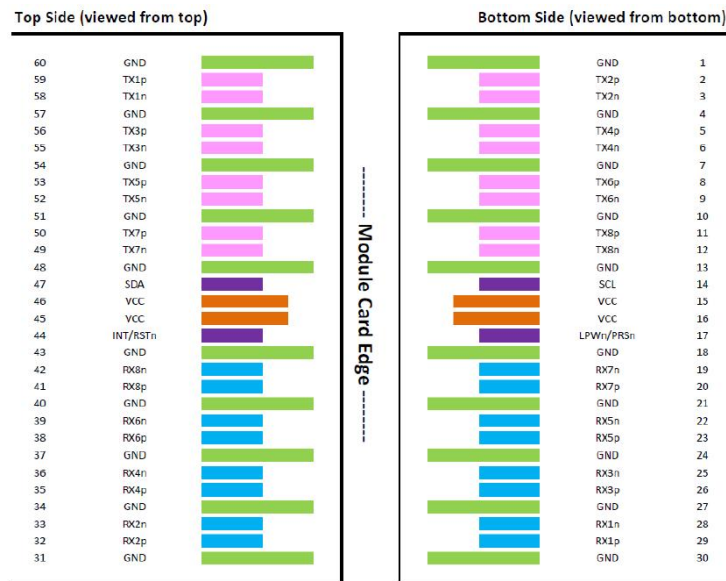


Figure 1 Pinout definitions of OSFP module inputs/outputs

## Pin Function Definitions

| Pin | Symbol     | Description                     | Logic       | Plug Sequence | Notes |
|-----|------------|---------------------------------|-------------|---------------|-------|
| 1   | GND        | Ground                          |             | 1             |       |
| 2   | TX2p       | Transmitter Data Non-Inverted   | CML-I       | 3             |       |
| 3   | TX2n       | Transmitter Data Inverted       | CML-I       | 3             |       |
| 4   | GND        | Ground                          |             | 1             |       |
| 5   | TX4p       | Transmitter Data Non-Inverted   | CML-I       | 3             |       |
| 6   | TX4n       | Transmitter Data Inverted       | CML-I       | 3             |       |
| 7   | GND        | Ground                          |             | 1             |       |
| 8   | TX6p       | Transmitter Data Non-Inverted   | CML-I       | 3             |       |
| 9   | TX6n       | Transmitter Data Inverted       | CML-I       | 3             |       |
| 10  | GND        | Ground                          |             | 1             |       |
| 11  | TX8p       | Transmitter Data Non-Inverted   | CML-I       | 3             |       |
| 12  | TX8n       | Transmitter Data Inverted       | CML-I       | 3             |       |
| 13  | GND        | Ground                          |             | 1             |       |
| 14  | SCL        | 2-wire Serial interface clock   | LVC MOS-I/O | 3             |       |
| 15  | VCC        | +3.3V Power                     |             | 2             |       |
| 16  | VCC        | +3.3V Power                     |             | 2             |       |
| 17  | LPWn/P RSn | Low-Power Mode / Module Present | Multi-Level | 3             |       |
| 18  | GND        | Ground                          |             | 1             |       |

|    |          |                                 |              |   |  |
|----|----------|---------------------------------|--------------|---|--|
| 19 | RX7n     | Receiver Data Inverted          | CML-0        | 3 |  |
| 20 | RX7p     | Receiver Data Non-Inverted      | CML-0        | 3 |  |
| 21 | GND      | Ground                          |              | 1 |  |
| 22 | RX5n     | Receiver Data Inverted          | CML-0        | 3 |  |
| 23 | RX5p     | Receiver Data Non-Inverted      | CML-0        | 3 |  |
| 24 | GND      | Ground                          |              | 1 |  |
| 25 | RX3n     | Receiver Data Inverted          | CML-0        | 3 |  |
| 26 | RX3p     | Receiver Data Non-Inverted      | CML-0        | 3 |  |
| 27 | GND      | Ground                          |              | 1 |  |
| 28 | RX1n     | Receiver Data Inverted          | CML-0        | 3 |  |
| 29 | RX1p     | Receiver Data Non-Inverted      | CML-0        | 3 |  |
| 30 | GND      | Ground                          |              | 1 |  |
| 31 | GND      | Ground                          |              | 1 |  |
| 32 | RX2p     | Receiver Data Non-Inverted      | CML-0        | 3 |  |
| 33 | RX2n     | Receiver Data Inverted          | CML-0        | 3 |  |
| 34 | GND      | Ground                          |              | 1 |  |
| 35 | RX4p     | Receiver Data Non-Inverted      | CML-0        | 3 |  |
| 36 | RX4n     | Receiver Data Inverted          | CML-0        | 3 |  |
| 37 | GND      | Ground                          |              | 1 |  |
| 38 | RX6p     | Receiver Data Non-Inverted      | CML-0        | 3 |  |
| 39 | RX6n     | Receiver Data Inverted          | CML-0        | 3 |  |
| 40 | GND      | Ground                          |              | 1 |  |
| 41 | RX8p     | Receiver Data Non-Inverted      | CML-0        | 3 |  |
| 42 | RX8n     | Receiver Data Inverted          | CML-0        | 3 |  |
| 43 | GND      | Ground                          |              | 1 |  |
| 44 | INT/RSTn | Module Interrupt / Module Reset | Multi- Level | 3 |  |
| 45 | VCC      | +3.3V Power                     |              | 2 |  |
| 46 | VCC      | +3.3V Power                     |              | 2 |  |
| 47 | SDA      | 2-wire Serial interface data    | LVCM OS-I/O  | 3 |  |
| 48 | GND      | Ground                          |              | 1 |  |
| 49 | TX7n     | Transmitter Data Inverted       | CML-I        | 3 |  |
| 50 | TX7p     | Transmitter Data Non-Inverted   | CML-I        | 3 |  |
| 51 | GND      | Ground                          |              | 1 |  |
| 52 | TX5n     | Transmitter Data Inverted       | CML-I        | 3 |  |
| 53 | TX5p     | Transmitter Data Non-Inverted   | CML-I        | 3 |  |
| 54 | GND      | Ground                          |              | 1 |  |
| 55 | TX3n     | Transmitter Data Inverted       | CML-I        | 3 |  |
| 56 | TX3p     | Transmitter Data Non-Inverted   | CML-I        | 3 |  |
| 57 | GND      | Ground                          |              | 1 |  |
| 58 | TX1n     | Transmitter Data Inverted       | CML-I        | 3 |  |

|    |      |                               |       |   |  |
|----|------|-------------------------------|-------|---|--|
| 59 | TX1p | Transmitter Data Non-Inverted | CML-I | 3 |  |
| 60 | GND  | Ground                        |       | 1 |  |

## Block Diagram of Transceiver

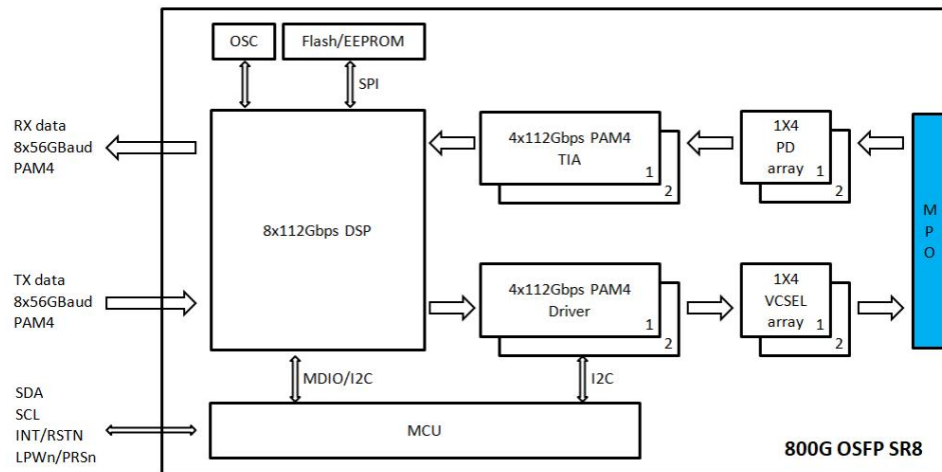


Figure 2 Block Diagram of Transceiver

## Recommended Interface Circuit Dimensions

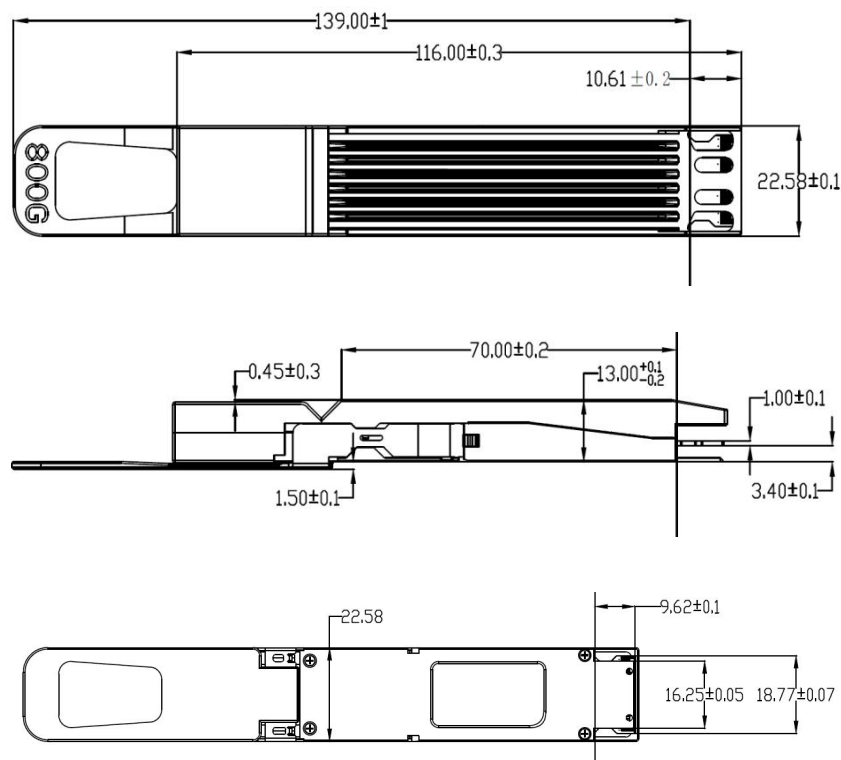


Figure 3 Recommended Interface Circuit Dimensions

## Digital Diagnostic Memory Map

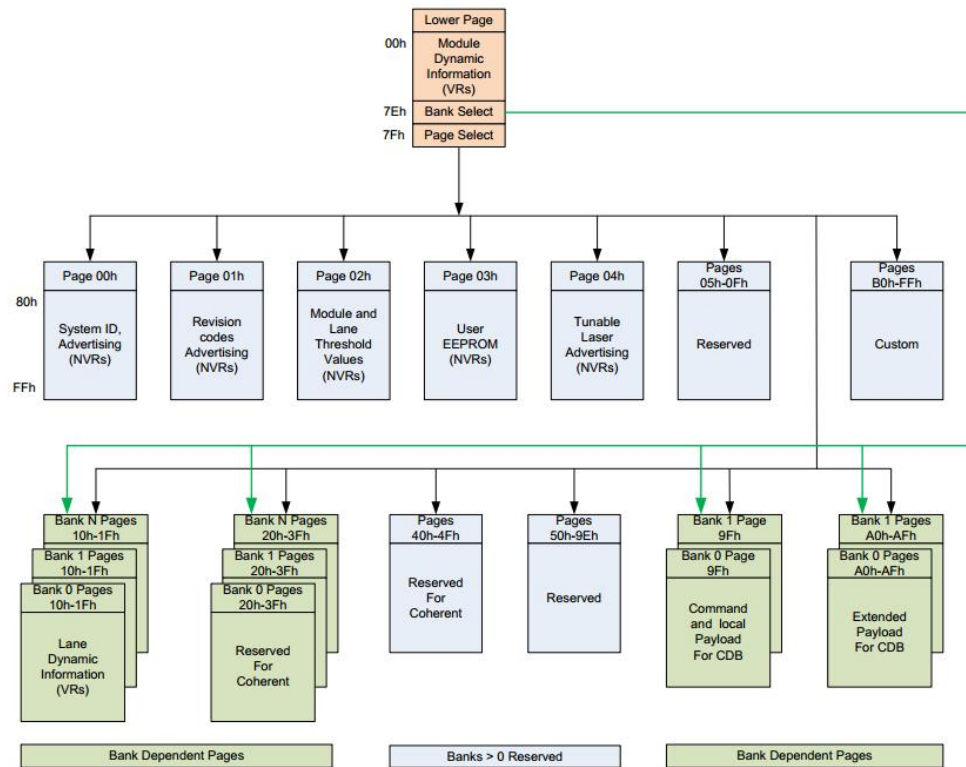


Figure 4 Digital Diagnostic Memory Map



## Further Information:

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