40Gb/s QSFP+ LR4 1310nm 10km Optical Transceiver

Features

- Compliant to the industry standard SFF-8436 QSFP+ Transceiver Specification
- QSFP+ MSA compliant
- Supports 41.2Gb/s aggregate bit rate
- 4 CWDM lanes MUX/DEMUX design
- Up to 10km transmission on single mode fiber (SMF)
- Operating case temperature: 0 to 70℃
- Maximum power consumption 3.5W
- LC duplex connector
- RoHS 2.0 compliant

Applications

- 40GBASE-LR4 Ethernet Links
- Client-side 40G Telecom connections

Compliance

- IEEE802.3ba 40GBASE-LR4
- SFF-8436 QSFP Specification

General Description

QSFP-40G-LR4 is a transceiver module designed for 0km optical communication applications. The design is compliant to 40GBASE-LR4 of the IEEE P802.3ba standard. The module converts 4 inputs channels (ch) of 10Gb/s electrical data to 4 CWDM optical signals, and multiplexes them into a single channel for 40Gb/s optical transmission. Reversely, on the receiver side, the module optically de-multiplexes a 40Gb/s input into 4 CWDM channels signals, and converts them to 4 channel output electrical data.

The central wavelengths of the 4 CWDM channels are 1271, 1291, 1311 and 1331nm as members of the CWDM wavelength grid defined in ITU-T G.694.2. It contains a duplex LC connector for the optical interface and a 148-pin connector for the electrical interface. To minimize the optical dispersion in the long-haul system, single-mode fiber (SMF) has to be applied in this module.

The product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP+ Multi-Source Agreement (MSA). It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference.

Functional Description

This product converts the 4-channel 10Gb/s electrical input data into CWDM optical signals (light), by a driven 4-wavelength Distributed Feedback Laser (DFB) array. The light is combined by the MUX parts as a 40Gb/s data, propagating out of the transmitter module from the SMF. The receiver module accepts the 40Gb/s CWDM optical signals input, and de-multiplexes it into 4 individual 10Gb/s channels with different wavelength. Each wavelength light is collected by a discrete photo diode, and then outputted as electric data after amplified first by a TIA and a post amplifier. Figure 1 shows the functional block diagram of this product.

A single +3.3V power supply is required to power up this product. Both power supply pins VccTx and VccRx are internally connected and should be applied concurrently. As per MSA specifications the module offers 7 low speed hardware control pins (including the 2-wire serial interface): ModSelL, SCL, SDA, ResetL, LPMode, ModPrsL and IntL.

Module Select (ModSelL) is an input pin. When held low by the host, this product responds to 2-wire serial communication commands. The ModSelL allows the use of this product on a single 2-wire interface bus – individual ModSelL lines must be used.

Serial Clock (SCL) and Serial Data (SDA) are required for the 2-wire serial bus communication interface and enable the host to access the QSFP+ memory map.

The ResetL pin enables a complete reset, returning the settings to their default state, when a low level on the ResetL pin is held for longer than the minimum pulse length. During the execution of a reset the host shall disregard all status bits until it indicates a completion of the reset interrupt. The product indicates this by posting an IntL (Interrupt) signal with the Data_Not_Ready bit negated in the memory map. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

Low Power Mode (LPMode) pin is used to set the maximum power consumption for the product in order to protect hosts that are not capable of cooling higher power modules, should such modules be accidentally inserted.

Module Present (ModPrsL) is a signal local to the host board which, in the absence of a product, is normally pulled up to the host Vcc. When the product is inserted into the connector, it completes the path to ground through a resistor on the host board and asserts the signal. ModPrsL then indicates its present by setting ModPrsL to a "Low" state.

Interrupt (IntL) is an output pin. "Low" indicates a possible operational fault or a status critical to the host system. The host

identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled to the Host Vcc voltage on the Host board.

Absolute Maximum Ratings

Table1-Absolute Maximum Ratings

Parameter	Symbols	Min.	Typical	Max.	Unit	Notes
Storage Temperature	TSTG	-40		+85	°C	
3.3V Supply Voltage	V_{CC}	0		+3.6	V	
Operating Temperature	Top	0		70		
Operating Relative Humidity	RH	5		85	%	
Damage Threshold, each Lane	TH_d	3.4			dBm	

Recommended Operating Conditions

Table2-Recommended Operating Conditions

Parameter	Symbols	Min.	Typical	Max.	Unit	Notes
Operating Case Temperature	Tc	0		+70	°C	
3.3V Supply Voltage	VCC	3.135	3.3	3.465	V	
Data Rate, each Lane			10.3125	11.2	Gbps	
Logic Input Voltage High	Vih	2		Vcc+0.3	V	
Logic Input Voltage Low	Vil	0		0.8	V	
Fiber Length		0.02		10	km	

Electrical Characteristic

Table3-Electrical Characteristic

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Power Consumption				3.5	W	
Supply Current	Icc			1.1	A	1
Transmitter (each Lane)						
Data Rate, each lane			10.3125		Gbps	2
Differential Voltage pk-pk	V_{pp}			900	mV	
Input differential impedance	R_{in}		100		Ohm	
Differential Termination Resistance Mismatch				10	%	3
Receiver (each Lane)						
Data Rate, each lane			10.3125		Gbps	2
Output differential impedance	R_{out}		100		Ohm	

Differential Termination Resistance Mismatch				10	%	3
Differential output voltage	V_{out}, pp			900	mV	

Notes:

[1] Steady state.

[2] For 40GBASE-LR4 application.

[3] At 1 MHz.

Optical Characteristic

Table4-Optical Characteristic

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Transmitter						
Signal Speed per Lane	BR	10.3125±100ppm			Gb/s	
Wavelength Assignment	L0	1264.5	1271	1277.5	nm	
	L1	1284.5	1291	1297.5	nm	
	L2	1304.5	1311	1317.5	nm	
	L3	1324.5	1331	1337.5	nm	
Side Mode Suppression Ratio	SMSR	30			dB	
Total Average Launch Power	P_T			8.3	dBm	
Average Launch Power, each Lane	P_{AVG}	-7		2.3	dBm	
Difference in launch power between any two lanes (Average and OMA)				6.5	dB	
Launch power OFF per lane				-40	dBm	
TDP, each Lane	TDP			2.6	dB	
Transmitter OFF Output Power	P_{off}			-30	dBm	
Optical Modulation Amplitude minus TDP, each lane		-4.8			dBm	
Extinction Ratio	ER	3.5			dB	
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}		{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}				1
Mask margin		15			%	1
Receiver (each Lane)						
Signal Speed per Lane	BR	10.3125±100ppm			Gb/s	
Wavelength Assignment	L0	1264.5	1271	1277.5	nm	
	L1	1284.5	1291	1297.5	nm	

	L2	1304.5	1311	1317.5	nm	
	L3	1324.5	1331	1337.5	nm	
Damage Threshold, each Lane	P_{min}	3.3			dBm	
Average Receive Power, each Lane		-13.7		2.3	dBm	
Receiver Sensitivity (OMA), each Lane	SEN			-11.5	dBm	2
Receive Power (OMA), each Lane				3.5	dBm	
Receiver Reflectance	R_R			-26	dB	
LOS Assert	LOSA	-30			dBm	
LOS Deassert	LOSD			-12.5	dBm	
LOS Hysteresis	LOSH	0.5		6	dB	

Notes:

[1] Hit ratio 5×10^{-5}.

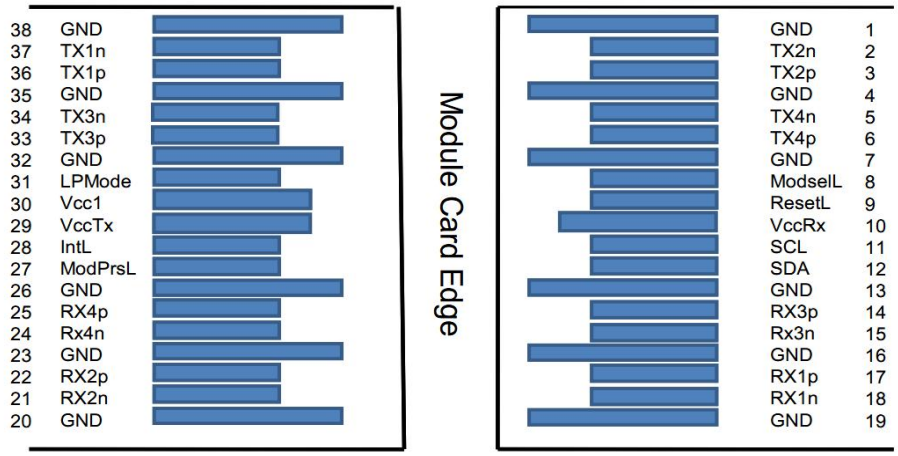
[2] Sensitivity is specified at BER@1E-12.

Digital Diagnostic Functions

Table5-Recommended Operating Conditions

Parameter	Accuracy	Unit
Case Temperature	±3	℃
Supply Voltage	±3%	V
Tx Bias Current	±10%	mA
Tx Optical Power	±3	dB
Rx Optical Power	±3	dB

Pin Description



Top Side
Viewed from Top

Bottom Side
Viewed from Bottom

Figure 1 Pin view

Pin Function Definitions

Table6-Pin Function Definitions

Pin	Symbol	Description	Note
1	GND	Ground	1
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data Input	
4	GND	Ground	1
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data Input	
7	GND	Ground	1
8	ModSelL	Module Select	
9	ModSelL	Module Select	
10	Vcc Rx	+3.3V Power Supply Receiver	2
11	SCL	2-wire serial interface clock	
12	SDA	2-wire serial interface data	
13	GND	Ground	1
14	Rx3p	Receiver Non-Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	
16	GND	Ground	1
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1p	Receiver Inverted Data Output	
19	GND	Ground	1

20	GND	Ground	1
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Ground	
24	Rx4n	Receiver Inverted Data Output	
25	Rx4p	Receiver Non-Inverted Data Output Ground	
26	GND	Ground	1
27	ModPrsL	Module Present	
28	IntL	Interrupt	
29	Vcc Tx	+3.3V Power supply transmitter	2
30	Vcc1	+3.3V Power supply	2
31	LPMode	Low Power Mode	
32	GND	Ground	1
33	Tx3p	Transmitter Non-Inverted Data Input	
34	Tx3n	Transmitter Inverted Data Input	
35	GND	Ground	1
36	Tx1p	Transmitter Non-Inverted Data Input	
37	Tx1n	Transmitter Inverted Data Input	
38	GND	Ground	1

Notes:

[1] GND is the symbol for signal and supply (power) common for the QSFP+ module. All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

[2] Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently.Recommended host board power supply filtering is shown in Figure 3. Vcc Rx Vcc1 and VccTx may be internally connected within the QSFP+ Module in any combination. The connector pins are each rated for a maximum current of 500 mA.

ModSelL Pin

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP modules on a single 2-wire interface bus. When the ModSelL is "High", the module will not respond to any 2-wire interface communication from the host. ModSelL has an internal pull-up in the module.

ResetL Pin

Reset. LPMode_Reset has an internal pull-up in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the xecution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module will post this completion of reset interrupt without requiring a reset.

LPMode Pin

This Pin operate in the low power mode (less than 1.5 W power consumption).

ModPrsL Pin

ModPrsL is pulled up to Vcc on the host board and grounded in the module. The ModPrsL is asserted "Low" when the module is inserted and de-asserted "High" when the module is physically absent from the host connector.

IntL Pin

IntL is an output pin. When "Low", it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt by using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled up to Vcc on the host board.

Recommended Power Supply Filter

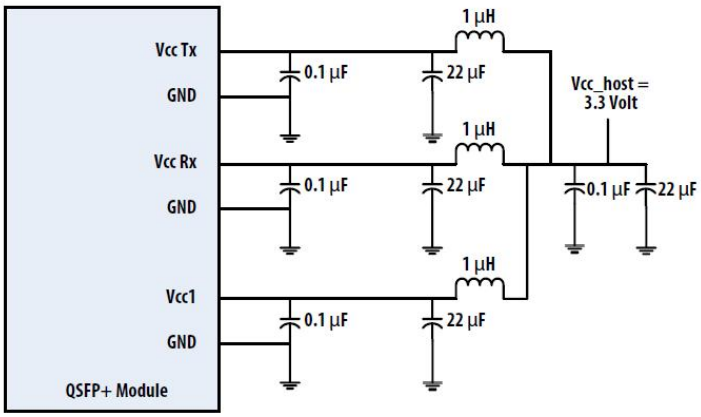


Figure 2 Recommended Power Supply Filter

Transceiver Block Diagram

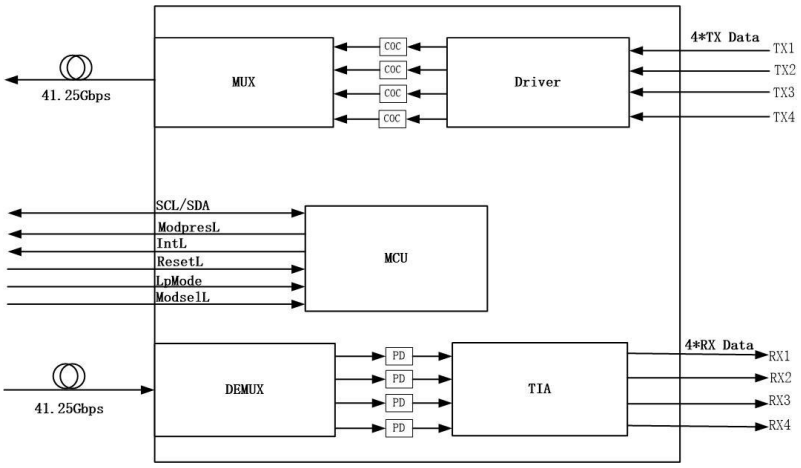


Figure 3 Transceiver Block Diagram

Mechanical Dimensions

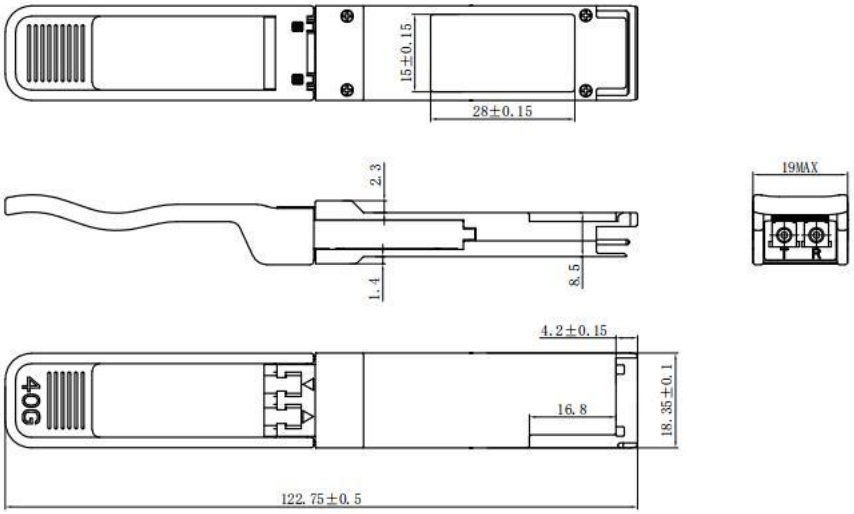


Figure 4 Mechanical Outline

Regulatory Compliance

Table7-Regulatory Compliance

Feature	Reference	Performance
EMC	EN61000-3	Compatible with standards
Electrostatic Discharge (ESD)	IEC/EN 61000-4-2	Compatible with standards
Electromagnetic Interference (EMI)	FCC Part 15 Class B EN 55022 Class B (CISPR 22A)	Compatible with standards
Laser Eye Safety	FDA 21CFR 1040.10, 1040.11 IEC/EN 60825-1, EC/EN 60825-2	Class 1 laser product
Component Recognition	IEC/EN 60950, L 60950	Compatible with standards
	2021/65/EU	Compatible with standards

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