800G Twin-port NDR Flat Top OSFP 2x400Gb/s Single Mode 2xDR4 100m Transceiver

Features

- OSFP MSA 5.0 compliant
- 8x106.25Gb/s PAM4 electrical interface
- EML transmitter and PIN PD receiver
- Maximum power consumption 16.5W@ Tcase = 70℃
- Compliant with OSFP MSA Specification Rev 5.0 RHS housing

  (with the longer body:107.8mm) with dual MPO-12/APC receptacle
- Up to 100m transmission on single mode fiber
- Operating case temperature: 0℃~70℃
- Single 3.3V power supply
- Hot pluggable, RoHS-6 compliant
- OSFP MSA Rev5.0
- IEEE 802.3ck, IEEE 802.3bs
- CMIS Rev5.2 compliant
- RoHS compliance

Applications

- The flat-top version offered for liquid-cooled and DGX H100 Cedar7 systems links

Description

The OSFP-800G-2xDR4FH is an InfiniBand and Ethernet 800Gb/s 2x400Gb/s Twin-port OSFP, 2xDR4 single mode, parallel, 8-channel transceiver using two, 4-channel MPO-12/APC optical connectors at 400Gb/s each. The parallel single mode, data center reach 8-channel (2xDR4) design uses 100G-PAM4 modulation and has a maximum fiber reach of 100-meters using 8 single mode fibers. The 100-meter length assumes two optical patch panels in the link.It has been designed to withstand the maximum range of external operating conditions including temperature, humidity and EMI. The module offers very high functionality and feature integration,accessible via a two-wire serial interface.

The Twin-port 2xDR4 transceiver is a key innovation with two internal transceiver engines enabling 64-ports of 400Gb/s in a 32-OSFP cage. The OSFP-800G-2xDR4FH is used in liquid-cooled and DGX-H100 systems.

Absolute Maximum Specifications

Absolute maximum ratings are those beyond which damage to the device may occur.

Prolonged operation between the operational specifications and absolute maximum ratings is not intended and may cause permanent device degradation.

Table1-Absolute Maximum Specifications

Parameter	Min.	Typical	Max.	Unit
Storage Temperature	-40		+85	°C
Supply Voltage	-0.5	3.3	3.6	V
Relative Humidity (non- condensing)	5		95	%
Data Input Voltage Differential			1	V
Control Input Voltage	-0.3		VCC+0.5	V
Control Output Current	-20		20	mA

Table2-Recommended Operating Conditions

Parameter	Min.	Typical	Max.	Unit
Operating Case Temperature	0		70	°C
Power Supply Voltage	3.135	3.3	3.465	V
Instantaneous peak current at hot plug			6600	mA
Sustained peak current at hot plug			5494.5	mA
Module Power Dissipation			16.5	W
Maximum Power Dissipation, Low Power Mode			2	W
Signalling Speed per Lane		53.125		GBd
Control Input Voltage High	Vcc*0.7		Vcc+0.3	V
Control Input Voltage Low	-0.3		Vcc*0.3	V
Two Wire Serial Interface Clock Rate			400	kHz
Power Supply Noise 1 kHz - 1 MHz (p-p)			66	mVpp

Operating Distance	2		100	m

Functional Characteristics (Optical)

Table3-Transmitter Operating Characteristic-Optical

Parameter	Symbol	Min.	Typical	Max.	Units
Optical Data Rate, each Lane			53.125±100ppm		GBd
Modulation Format			PAM4		
Wavelength	λC	1304.5	1311	1317.5	nm
Side Mode Suppression Ratio	SMSR	30	-	-	dB
Average Launch Power, each lane	AOPL	-2.9	-	4.0	dBm
Outer Optical Modulation Amplitude (OMAouter), each Lane	TOMA	-0.8	-	4.2	dBm
Launch power in OMAouter minus TDECQ, each lane for extinction ratio >= 5 dB for extinction ratio<5 dB	TOMA-TDECQ	-2.2 -1.9			dBm
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each lane	TDECQ	-	-	3.4	dB
TDECQ – 10log10(Ceq), each lane	Ceq			3.4	dB
Average Launch Power of OFF Transmitter, each lane	T_{OFF}			-15	dBm
Extinction Ratio	ER	3.5			dB
Transmitter transition time	Tr			17	ps
$RIN_{15.5}OMA$	RIN			-136	dB/Hz
Optical return loss tolerance	ORL			15.5	dB
Transmitter Reflectance	T_R			-26	dB

Table4-Receiver Operating Characteristic-Optical

Parameter	Symbol	Min.	Typical	Max.	Unit	Note
Wavelength	λC0	1304.5	1311	1317.5	nm	
Damage Threshold, each Lane	AOPD	5	-	-	dBm	
Average Receive Power, each Lane	AOPR	-5.9	-	4	dBm	
Receive Power (OMAouter), each Lane	OMAR	-	-	4.2	dBm	
Receiver Reflectance	RR	-	-	-26	dB	
Receiver Sensitivity (OMAouter), each Lane	SOMA	-	-	Max(-3.9, SECQ – 5.3)	dBm	1
Stressed Receiver Sensitivity (OMAouter), each Lane	SRS	-	-	-1.9	dBm	2
Conditions of stressed receiver sensitivity						

test						
Stressed eye closure for PAM4 (SECQ), lane under test	SECQ	-	3.4	-	dB	
SECQ – 10log10(Ceq), lane under test	Ceq	-	-	3.4	dB	

Notes:

[1] Receiver sensitivity (OMAouter), each lane (max) is informative and is defined for a transmitter with a value of SECQ up to 3.4 dB.

[2] Measured with conformance test signal at TP3 for the BER = 2.4x10-4.

Functional Characteristics (Electrical)

Table5-Transmitter Operating Characteristic-Electrical

Parameter	Symbol	Min.	Typical	Max.	Units
Differential pk-pk input Voltage tolerance (TP1a)	-	750	-	-	
Peak-to-peak AC common-mode voltage tolerance Low-frequency, VCMLF Full-band, VCMFB	-	-	-	32 80	
Differential-mode to common-mode return loss	RLcd		802.3ck 120G-2		
Effective return loss	ERL	8.5	-	-	
Differential termination mismatch	-	-	-	10	
Single-ended voltage tolerance range	-	-0.4	-	3.3	
DC common-mode voltage tolerance	-	-0.35	-	2.85	

Table6-Receiver Operating Characteristic-Electrical

Parameter	Symbol	Min.	Typical	Max.	Units
Peak-to-peak AC common-mode voltage Low-frequency, VCMLF Full-band, VCMFB	-	-	-	32 80	mV
Differential peak-to-peak output voltage Short mode Long mode	-	-	-	600 845	mV
Eye height	EH	15	-	-	mV
Vertical eye closure	VEC	-	-	12	dB
Common-mode to differential-mode return loss	RLDc		802.3ck 120G-1		dB
Effective return loss	ERL	8.5	-	-	dB
Differential termination mismatch	-	-	-	10	%
Transition time	-	8.5	-	-	ps
DC common-mode voltage tolerance	-	-0.35	-	2.85	V

Electrical Specification Low Speed Control and Sense Signals

Table7-Electrical Specification Low Speed Control and Sense Signals

Parameter	Symbol	Min.	Max.	Unit	Condition
Module output SCL and SDA	VOL	0	0.4	V	
Module Input SCL and SDA	VIL	-0.3	VCC*0.3	V	
	VIH	VCC*0.7	VCC+0.5	V	
InitMode, ResetL and ModSelL	VIL	-0.3	0.8	V	
	VIH	2	VCC+0.3	V	
IntL	VOL	0	0.4	V	
	VOH	VCC-0.5	VCC+0.3	V	

Pin Description

Table8-Pin Description

Pin	Symbol	Description	Pin	Symbol	Description
1	GND	Ground	31	GND	Ground
2	Tx2p	Transmitter Non-Inverted Data Input	32	Rx2p	Receiver Non-Inverted Data Output
3	Tx2n	Transmitter Inverted Data Input	33	Rx2n	Receiver Inverted Data Output
4	GND	Ground	34	GND	Grounds
5	Tx4p	Transmitter Non-Inverted Data Input	35	Rx4p	Receiver Non-Inverted Data Output
6	Tx4n	Transmitter Inverted Data Input	36	Rx4n	Receiver Inverted Data Output
7	GND	Ground	37	GND	Ground
8	Tx6p	Transmitter Non-Inverted Data Input	38	Rx6p	Receiver Non-Inverted Data Output
9	Tx6n	Transmitter Inverted Data Input	39	Rx6n	Receiver Inverted Data Output
10	GND	Ground	40	GND	Ground
11	Tx8p	Transmitter Non- Inverted Data input	41	Rx8p	Receiver Non-Inverted Data Output
12	Tx8n	Transmitter Inverted Data Input	42	Rx8n	Receiver Inverted Data Output
13	GND	Ground	43	GND	Ground
14	SCL	2-wire serial interface clock	44	INT / RSTn	Module Interrupt / Module Reset
15	VCC	+3.3V Power	45	VCC	+3.3V Power
16	VCC	+3.3V Power	46	VCC	+3.3V Power
17	LPWn / PRSn	Low-Power Mode / Module Present	47	SDA	2-wire Serial interface data
18	GND	Ground	48	GND	Ground
19	Rx7n	Receiver Inverted Data Output	49	Tx7n	Transmitter Inverted Data Input

20	Rx7p	Receiver Non-Inverted Data Output	50	Tx7p	Transmitter Non-Inverted Data Input
21	GND	Ground	51	GND	Ground
22	Rx5n	Receiver Inverted Data Output	52	Tx5n	Transmitter Inverted Data Input
23	Rx5p	Receiver Non-Inverted Data Output	53	Tx5p	Transmitter Non-Inverted Data Input
24	GND	Ground	54	GND	Ground
25	Rx3n	Receiver Inverted Data Output	55	Tx3n	Transmitter Inverted Data Input
26	Rx3p	Receiver Non-Inverted Data Output	56	Tx3p	Transmitter Non-Inverted Data Input
27	GND	Ground	57	GND	Ground
28	Rx1n	Receiver Inverted Data Output	58	Tx1n	Transmitter Inverted Data Input
29	Rx1p	Receiver Non-Inverted Data Output	59	Tx1p	Transmitter Non-Inverted Data Input
30	GND	Ground	60	GND	Ground

OSFP Module Pad Layout

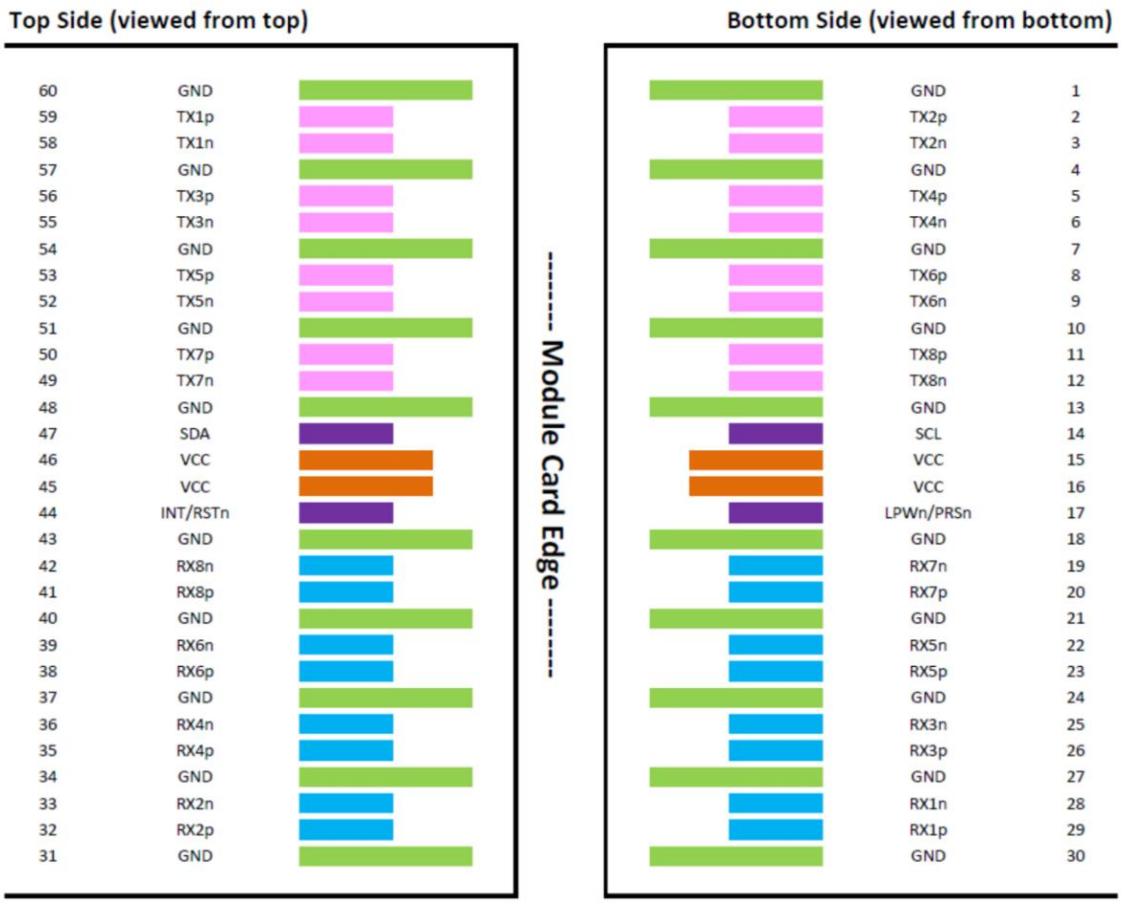

Figure1 OSFP module pin out

Block Diagram of Transceiver

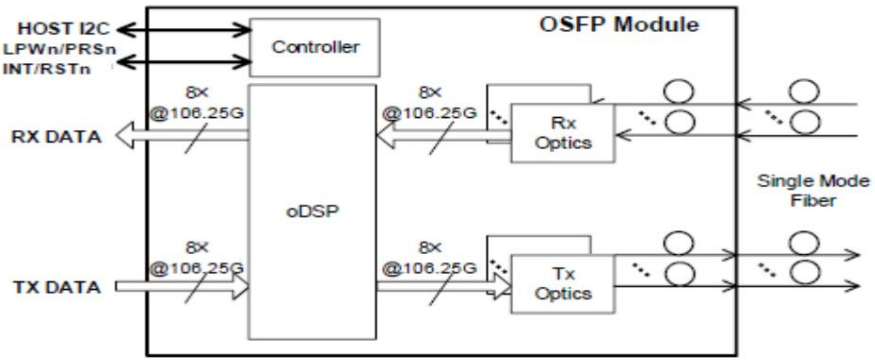

Figure2 Diagram of Transceiver

＜Transmitter Section＞: The OSFP 800G 2xDR4 converts 8-channel 106.25Gb/s electrical data to 8-channel 1311nm 106.25Gb/s optical signals for 850Gb/s optical transmission.

＜Receiver Section＞: Similarly, it optically converts 8-channel 1311nm 106.25Gb/s optical signals to 8-channel electrical data output on the receiver side.

Recommended OSFP Host Board Schematic

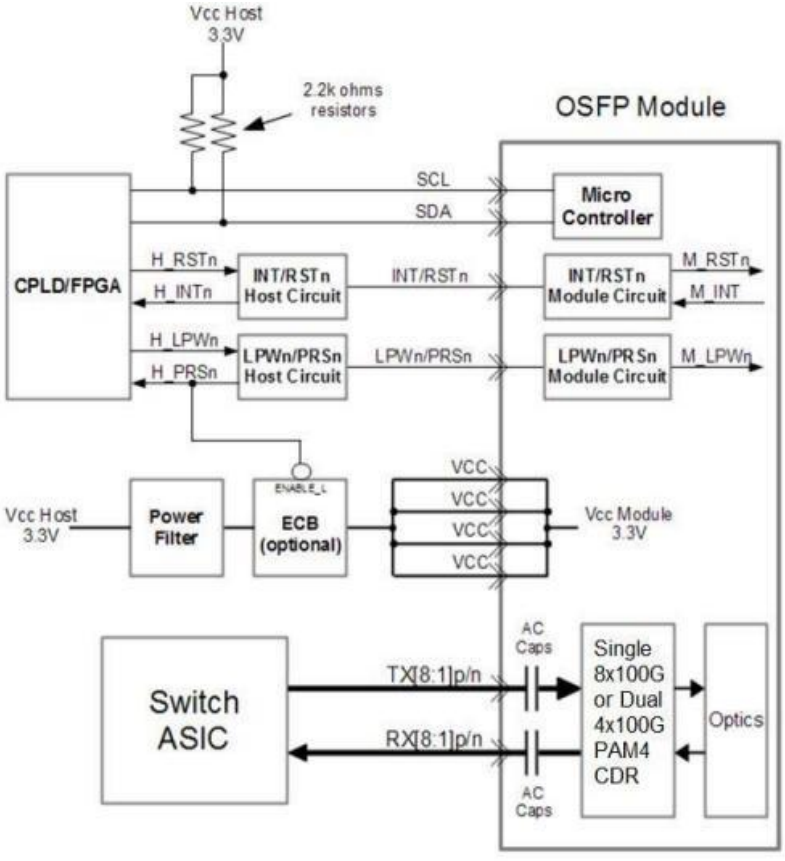

Figure3 Recommended OSFP Host Board Schematic

Digital Diagnostics

Table9-Digital Diagnostics

Parameter	Range	Accuracy	Unit	Calibration
Temperature	0 to 70	±3	°C	Internal
Voltage	0 to VCC	0.1	V	Internal
Tx Bias Current (Each Lane)	0 to 100	10%	mA	Internal
Tx Output Power (Each Lane)	-2.9 to +4	±3	dB	Internal
Rx Receive Power (Each Lane)	-5.9 to +4	±3	dB	Internal

Mechanical Diagram

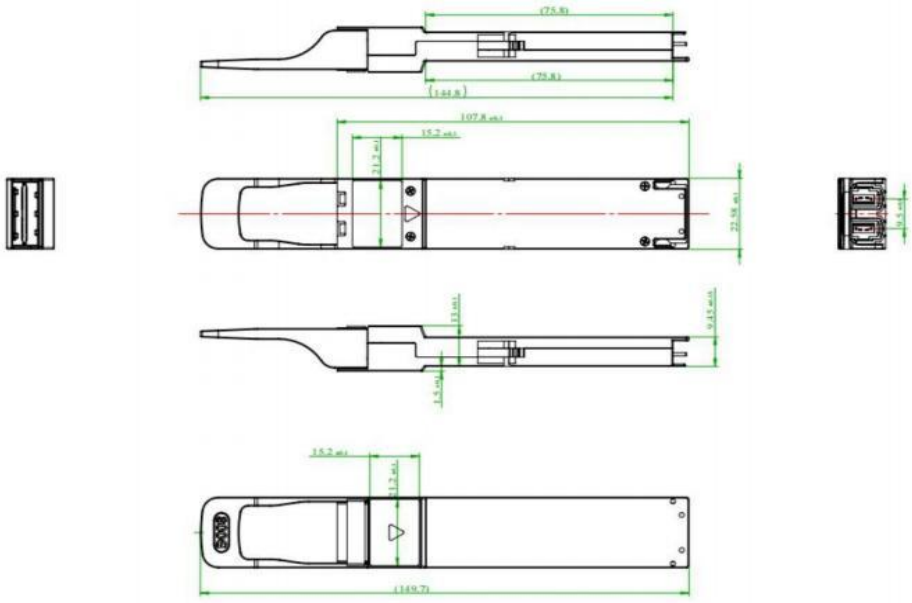

Figure4 Mechanical Diagram

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