800G Twin-port NDR OSFP 2x400Gb/s Multimode 2xSR4 50m Transceiver

Features

- InfiniBand and Ethernet
- 800G 2xSR4 multimode transceiver
- 8-channels of 100G-PAM4 electrical modulation
- Two ports of 4-channel 100G-PAM4 optical modulation
- Supports two straight 400Gb/s or two 1:2 splitter fiber cables for 200Gb/s
- Flat-top OSFP for DGX- H100 or liquid-cooled
- 850nm VCSEL
- Maximum reach: 30m using OM3 fiber / 50m using OM4 fiber
- Two MPO-12/APC optical connectors
- 14 Watts max power
- Single 3.3V power supply
- Class 1 laser safety
- Hot pluggable, RoHS compliant
- CMIS 4.0 compliant
- Case temperature range 0°C to +70°C

Description

The OSFP-800G-2SR4FH is an InfiniBand and Ethernet 800Gb/s 2x400Gb/s Twin-port OSFP, 2xSR4 multimode, parallel, 8-channel transceiver using two, 4-channel MPO-12/APC optical connectors at 400Gb/s each. The parallel multimode, short reach 8-channel (2xSR4) uses 100G-PAM4 modulation and has a maximum fiber reach of 50-meters using 8 multimode fibers.

The Quantum-2 and Spectrum-4 switches require finned-top OSFP shells for extra transceiver cooling. A flat-top version offered for liquid-cooled and DGX H100 Cedar7 systems links.

The transceiver combinations guarantee optimal operation. Rigorous production testing ensures the best out-of-the-box installation experience, performance, and durability

Absolute Maximum Specifications

Absolute maximum ratings are those beyond which damage to the device may occur.
Prolonged operation between the operational specifications and absolute maximum ratings is not intended and may cause permanent device degradation.

Table1-Absolute Maximum Specifications

Parameter	Min.	Typical	Max.	Unit	Note
Storage Temperature	-40		+85	°C	
Supply voltage	-0.5		3.6	V	
Relative Humidity (non- condensing)	0		85	%	
Control input voltage	-0.3		Vcc+0.5	V	
Operating Case Temperature	0		70	°C	

Recommended Operating Conditions

Table2-Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max.	Units	Notes
Operating Case Temperature	TOP	0		70	degC	
Power Supply Voltage	VCC	3.135	3.3	3.465	V	
Data Rate, each Lane			53.125		GBd	
Data Rate Accuracy		-100		100	ppm	
Pre-FEC Bit Error Ratio				$2.4x10^{-4}$		
Post-FEC Bit Error Ratio				$1x10^{-15}$		1
Link Distance (OM4)	D1	2		50	m	2
Link Distance (OM3)	D2	2		30	m	

Notes:

[1] FEC provided by host system.

[2] FEC required on host system to support maximum distance.

Electrical Specifications

Table3-Electrical Specifications

Parameter	Test Point	Min.	Typical	Max.	Unit	Note
Power Consumption				14	W	
Supply Current	Icc			4.24	A	
Module Input (each Lane)						
Signaling Rate, each Lane	TP1		53.125 ± 100 ppm		GBd	
DC Common-mode input Voltage	TP1	-0.35		2.85	V	
Single-ended input Voltage	TP1a	-0.4		3.3	V	
AC common-mode voltage tolerance Low-frequency, VCMLF Full-band, VCMLF	TP1a	 32 80			mV	
Module stressed input tolerance	TP1a		IEEE 802.3ck D3.3 120G.3.4.3			
Differential Peak-to-Peak input Voltage tolerance	TP1a	750			mV	
Differential to common-mode return loss, RLcd	TP1		IEEE 802.3ck D3.3 Equation 120G-2		dB	
Effective return loss, ERL	TP1	8.5			dB	
Differential termination mismatch	TP1			10	%	
Module Output (each Lane)						
Signaling Rate, each lane	TP4		53.125 ± 100 ppm		GBd	
Peak-to-peak AC common-mode voltage Low-frequency, VCMLF Full-band, VCMLF	TP4			 32 80	mV	
Differential peak-to-peak output voltage Short mode Long mode	TP4			 600 845	mV	
Eye height	TP4	15			mV	
Vertical eye closure, VEC	TP4			12	dB	
Common-mode to differential return loss, RLdc	TP4		IEEE 802.3ck Equation 120G-1		dB	
Effective return loss, ERL	TP4	8.5			dB	
Differential termination mismatch	TP4			10	%	
Transition time	TP4	8.5			ps	

DC common-mode voltage tolerance	TP4	-0.35		2.85	V	

Electrical Specification for Low Speed Signal

Table4-Electrical Specification for Low Speed Signal

Parameter	Symbol	Min.	Max	Units
Module output SCL and SDA	VOL	0	0.4	V
	VOH	VCC-0.5	VCC+0.3	V
Module Input SCL and SDA	VIL	-0.3	VCC*0.3	V
	VIH	VCC*0.7	VCC+0.5	V

Optical Specifications

Table5-Optical Specifications

Parameter	Symbol	Min.	Typical	Max.	Unit	Note
Transceiver						
Wavelength	λ C	844	850	863	nm	
RMS spectral width	Dl			0.6		
Average Launch Power, each lane	PAVG	-4.6	-	4.0	dBm	1
Outer Optical Modulation Amplitude (OMAouter), each lane (min)	TOMA	-2.1		3.5	dBm	2
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each lane	TDECQ	-	-	4.4	dB	
Average Launch Power of OFF Transmitter, each lane	TOFF	-	-	-30	dBm	
Extinction Ratio, each lane	ER	2.5		3.5	dB	
RIN14OMA	RIN	-	-148		dB/Hz	
Optical Return Loss Tolerance	ORLT		-	14	dB	
Transmitter Reflectance	TR	-	-	-26	dB	3
Receiver						
Wavelength	λ C	842	850	863	nm	
Damage Threshold, average optical power, each lane	AOPD	5	-	-	dBm	
Average Receive Power, each lane	AOPR	-6.4	-	4.0	dBm	6
Receive Power (OMAouter), each lane	OMA-R	-	-	3.5	dBm	
Receiver Reflectance	RR	-	-	-20	dB	
Receiver Sensitivity (OMAouter), each lane	SOMA	-	-	-4.6	dBm	4
Stressed Receiver Sensitivity	SRS	-	-	-2.0	dBm	5

(OMAouter), each lane						
Conditions of stressed receiver sensitivity test						
Stressed eye closure for PAM4	SECQ		4.4		dB	
OMAouter of each aggressor lane	OMAouter		3.5		dBm	

Notes:

[1] Average launch power, each lane (min) is informative and not the principal indicator signal strength.

[2] Even if max(TECQ,TDECQ) < 1.8dB, OMAouter (min) must exceed this value.

[3] Transmitter reflectance is defined looking into the transmitter.

[4] Receiver sensitivity (OMAouter), each lane (max) is informative and is defined for a transmitter with TDECQ<=1.8 dB

[5] Measured with conformance test signal at TP3 for the BER = $2.4x10^{-4}$

[6] Minimum power is informative. AOP above the minimum does not ensure compliance

Pin Description

The device is OSFP MSA Specification for OSFP Octal Small Form Factor Pluggable Module Rev. 1.12 compliant, see www.osfpmsa.org.

Table6-Pin Description

Pin	Symbol	Description	Pin	Symbol	Description
1	GND	Ground	31	GND	Ground
2	Tx2p	Transmitter Non-Inverted Data Input	32	Rx2p	Receiver Non-Inverted Data Output
3	Tx2n	Transmitter Inverted Data Input	33	Rx2n	Receiver Inverted Data Output
4	GND	Ground	34	GND	Grounds
5	Tx4p	Transmitter Non-Inverted Data Input	35	Rx4p	Receiver Non-Inverted Data Output
6	Tx4n	Transmitter Inverted Data Input	36	Rx4n	Receiver Inverted Data Output
7	GND	Ground	37	GND	Ground
8	Tx6p	Transmitter Non-Inverted Data Input	38	Rx6p	Receiver Non-Inverted Data Output
9	Tx6n	Transmitter Inverted Data Input	39	Rx6n	Receiver Inverted Data Output
10	GND	Ground	40	GND	Ground
11	Tx8p	Transmitter Non- Inverted Data input	41	Rx8p	Receiver Non-Inverted Data Output
12	Tx8n	Transmitter Inverted Data Input	42	Rx8n	Receiver Inverted Data Output
13	GND	Ground	43	GND	Ground
14	SCL	2-wire serial interface clock	44	INT / RSTn	Module Interrupt / Module Reset
15	VCC	+3.3V Power	45	VCC	+3.3V Power
16	VCC	+3.3V Power	46	VCC	+3.3V Power
17	LPWn / PRSn	Low- Power Mode / Module Present	47	SDA	2-wire Serial interface data

18	GND	Ground	48	GND	Ground
19	Rx7n	Receiver Inverted Data Output	49	Tx7n	Transmitter Inverted Data Input
20	Rx7p	Receiver Non-Inverted Data Output	50	Tx7p	Transmitter Non-Inverted Data Input
21	GND	Ground	51	GND	Ground
22	Rx5n	Receiver Inverted Data Output	52	Tx5n	Transmitter Inverted Data Input
23	Rx5p	Receiver Non-Inverted Data Output	53	Tx5p	Transmitter Non-Inverted Data Input
24	GND	Ground	54	GND	Ground
25	Rx3n	Receiver Inverted Data Output	55	Tx3n	Transmitter Inverted Data Input
26	Rx3p	Receiver Non-Inverted Data Output	56	Tx3p	Transmitter Non-Inverted Data Input
27	GND	Ground	57	GND	Ground
28	Rx1n	Receiver Inverted Data Output	58	Tx1n	Transmitter Inverted Data Input
29	Rx1p	Receiver Non-Inverted Data Output	59	Tx1p	Transmitter Non-Inverted Data Input
30	GND	Ground	60	GND	Ground

OSFP Module Pad Layout

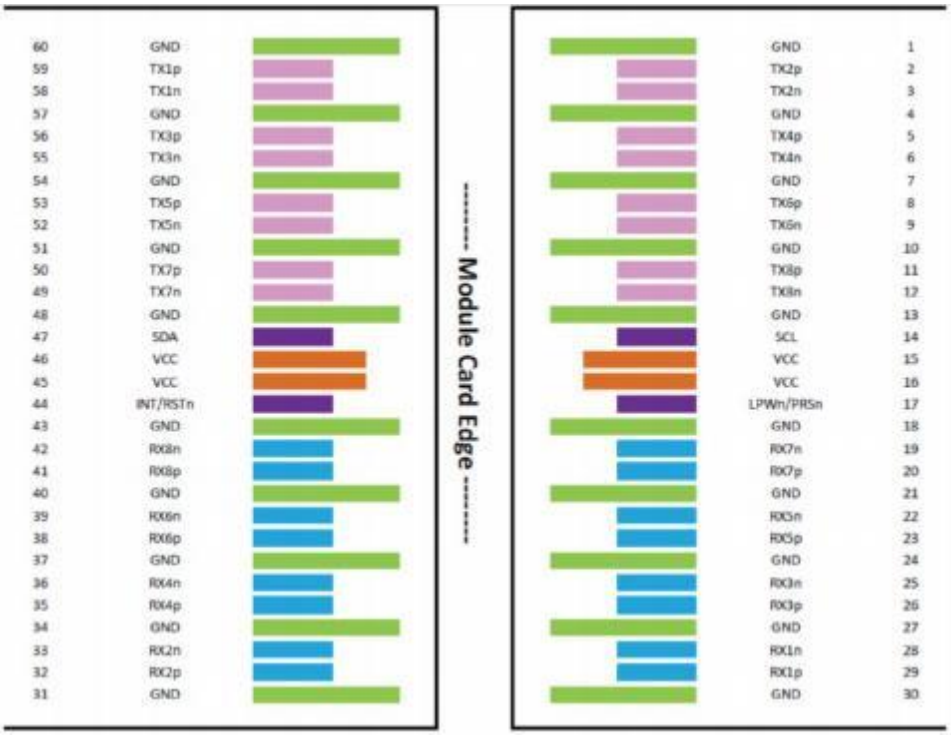

Figure 1 MSA Compliant Connector

Transceiver Block Diagram

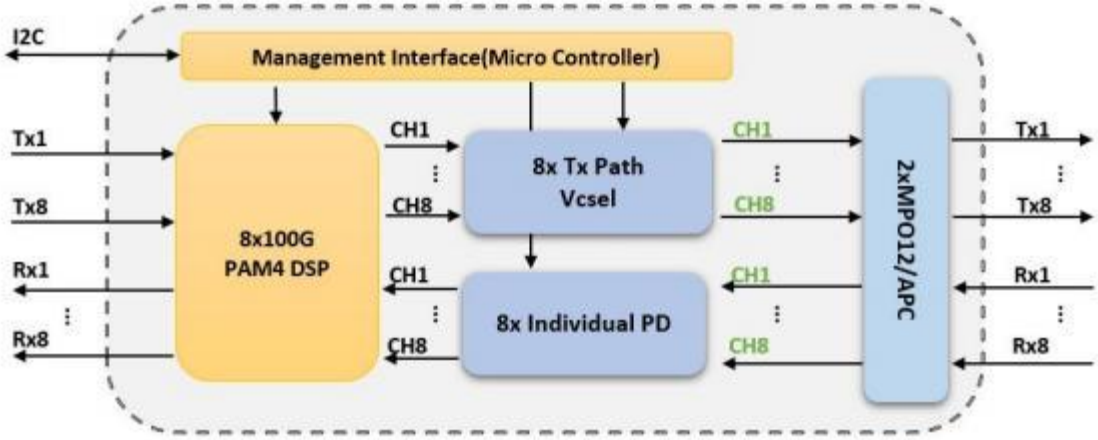

Figure 2. Transceiver Block Diagram

Optical Port Description

The optical interface port is dual MPO-12 APC receptacle. The transmit and receive optical lanes shall occupy the positions depicted in Figure 3 when looking into the MDI receptacle with the connector key way feature on top.

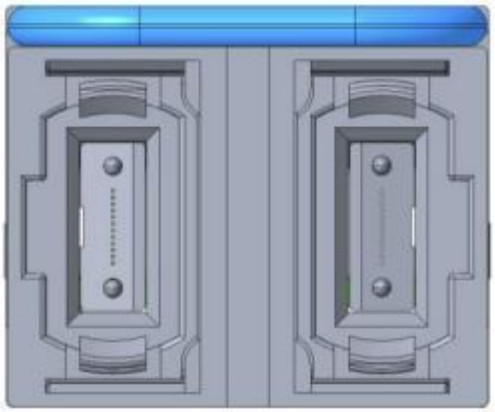

Figure 3 Optical Media Dependent Interface port assignments

Mechanical Drawing

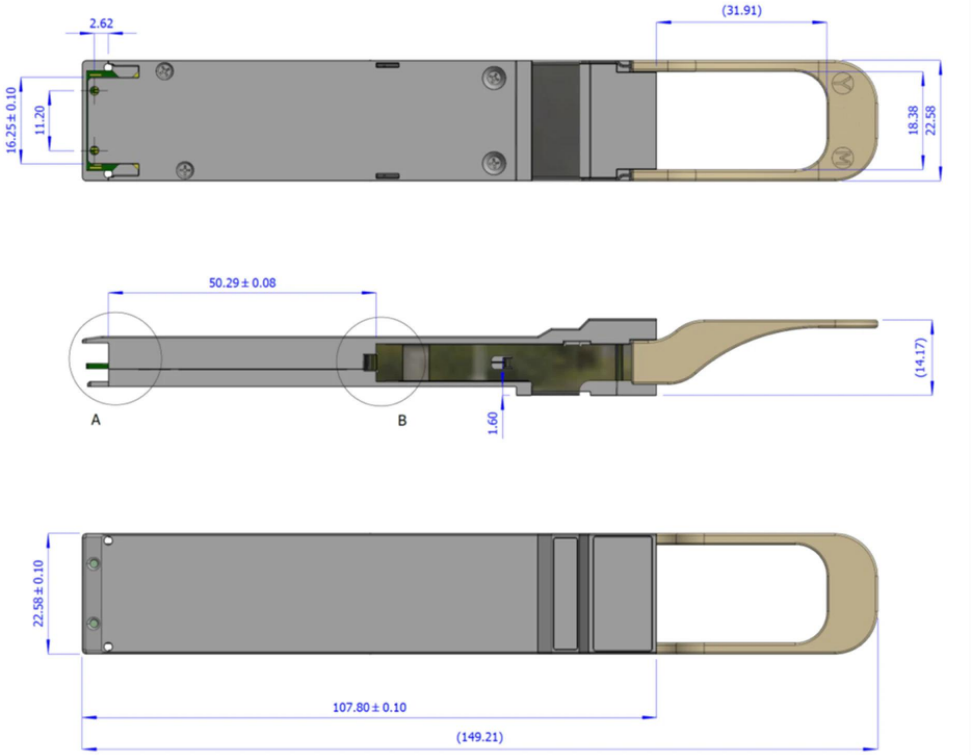

Figure 4 Mechanical Outline

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