800Gb/s QSFP-DD 2xDR4 1310nm 500m Optical Transceiver

Features

- Compliant with IEEE 802.3cu-2021: - 8x100GBASE-DR optical Interface
- Compliant with IEEE P802.3ck-2022: -8x100GAUI-1 C2M electrical interface
- Compliant with QSFP-DD MSA HW Rev 7.0 Type 2B with Dual MPO-12 APC connector
- Compliant with CMIS Rev 5.0
- Maximum Power Consumption 18w
- Operating Temperature Range: 0℃ ~ +70 ℃
- Two Wire Serial Interface with Digital Diagnostic Monitoring
- Complies with EU Directive 2011/65/EU (RoHS compliant)
- Class 1 Laser Safety

Applications

- 800G Ethernet
- Data Center
- Cloud Networks

Description

QDD-800G-2xDR4 is a high-speed optical module based on PAM4 modulation technology. It complies with QSFP-DD MSA and IEEE 802.3ck/802.3cu standards, supports a total transmission rate of 800Gbps, and integrates 2 independent 400G DR4 channels. Each channel realizes 4-channel 100G (4x100G PAM4) data transmission through an MPO-12 interface. This module is suitable for switches equipped with 800G QSFP-DD ports. It can be connected to 800G modules or two 400G DR4 QSFP-DD modules through MPO-12 APC fiber cables. It is widely used in data center Spine-Leaf architecture, AI clusters, high-performance computing centers, etc.

Absolute Maximum Ratings

Table1-Absolute Maximum Ratings

Parameter	Symbols	Min.	Typical	Max.	Unit	Notes
Storage Temperature	TS	-40		+85	°C	
Operating Relative Humidity (non-condensing)	R_H	5		95	%	
Supply Voltage	V_{CC}	-0.5		3.6	V	
Data Input Voltage Differential	IVDIP-VDIN			1	V	
Control Input Voltage	VI	-0.3		V_{CC}+0.5	V	
Control Output Current	IO	-20		20	mA	

Recommended Operating Conditions

Table2-Recommended Operating Conditions

Parameter	Symbols	Min.	Typical	Max.	Unit	Notes
Operating Case Temperature	Top	0		+70	℃	
Power Supply Voltage	VCC	3.135	3.3	3.465	V	
Instantaneous peak current at hot plug	ICC_IP			7200	mA	
Sustained peak current at hot plug	ICC_SP			5940	mA	
Maximum Power Dissipation	P_D			18	W	
Maximum Power Dissipation, Low Power Mode	P_{DLP}			2.5	W	
Signalling Speed per Lane	DRL		53.125		GBd	
Control Input Voltage High	VIH	VCC*0.7		VCC+0.3	V	
Control Input Voltage Low	VIL	-0.3		VCC*0.3	V	
Two Wire Serial Interface Clock Rate				400	kHz	
Power Supply Noise 1 kHz - 1 MHz (p-p)				66	mVpp	
Operating Distance		2		500	m	

Optical Characteristics

Table3-Optical Characteristics

Parameter	Symbols	Min.	Typical	Max.	Unit	Notes
Wavelength	λc	1304.5	1311	1317.5	nm	
			Transmitter			
Side Mode Suppression Ratio	SMSR	30			dB	
Average Launch Power, each lane	AOPL	-2.9		4.0	dBm	1
Outer Optical Modulation Amplitude (OMA_{outer}), each Lane	TOMA	-0.8		4.2	dBm	
Launch power in OMAouter minus TDECQ , each lane for extinction ratio ＞= 5 dB for extinction ratio ＜ 5 dB	$T_{OMA-TDECQ}$	 -2.2 -1.9			dBm	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each lane	TDECQ			3.4	dB	
TDECQ – 10log10(Ceq), each lane	Ceq			3.4	dB	
Average Launch Power of OFF Transmitter, each lane	TOFF			-15	dBm	
Extinction Ratio	ER	3.5			dB	
Transmitter transition time (max)	Tr			17	ps	
RIN21.4OMA (max)	RIN			-136	dB/Hz	
Optical Return Loss Tolerance	ORL			15.5	dB	
Transmitter Reflectance	TR			-26	dB	2
			Receiver			
Wavelength L0	$λ_{C0}$	1304.5	1311	1317.5	nm	
Damage Threshold, each Lane	AOP_D	5			dBm	
Average Receive Power, each Lane	AOP_R	-5.9		4	dBm	
Receive Power (OMA_{outer}), each Lane	OMA_R			4.2	dBm	
Receiver Reflectance	RR			-26	dB	
Receiver Sensitivity (OMA_{outer}), each Lane	SOMA			Max(–3.9, SECQ – 5.3)	dBm	3
Stressed Receiver Sensitivity (OMA_{outer}), each Lane	SRS			-1.9	dBm	4
Conditions of stressed receiver sensitivity test						
Stressed eye closure for	SECQ		3.4		dB	

PAM4(SECQ), lane under test						
SECQ–10log10(Ceq), lane under test	Ceq			3.4	dB	
OMA_{outer} of each aggressor lane			4.2			

Electrical Characteristic

Table4-Electrical Characteristic

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Transmitter						
Differential pk-pk input Voltage tolerance (TP1a)		750		25	mV	
Peak-to-peak AC common-mode voltage tolerance Low-frequency , VCMLF Full-band, VCMFB		32 80			mV	
Common-mode to differential return loss	RLDc		802.3ck 120G- 2		dB	
Effective return loss, ERL	ERL	8.5			dB	
Differential termination mismatch				10	%	
Single-ended voltage tolerance range		-0.4		3.3	V	
DC common-mode voltage tolerance		-0.35		2.85	V	
Receiver						
Peak-to-peak AC common-mode voltage Low-frequency , VCMLF Full-band, VCMFB				32 80	mV	
Differential peak-to-peak output voltage Short mode Long mode				600 845	mV	
Eye height	EH	15			mV	
Vertical eye closure	VEC			12	dB	
Differential to common-mode return loss	RLDc		802.3ck 120G-2		dB	
Effective return loss, ERL	ERL	8.5			dB	
Differential termination mismatch				10	%	
Transition time		8.5			ps	
DC common-mode volta e tolerance		-0.35		2.85	v	

Electrical Specification Low Speed Control and Sense Signals

Table5-Electrical Specification Low Speed Control and Sense Signals

Parameter	Symbols	Min.	Max.	Unit	Notes
Module output SCL and SDA	VOL	0	0.4	V	
Module Input SCL and SDA	VIL	-0.3	VCC*0.3	V	
	VIH	VCC*0.7	VCC+0.5	V	
LPMode/TxDis,ResetL and ModSelL	VIL	-0.3	0.8	V	
	VIH	2	VCC+0.3	V	
IntL/RxLos	VOL	0	0.4	V	
	VOH	VCC-0.5	VCC+0.3	V	

Pin Description

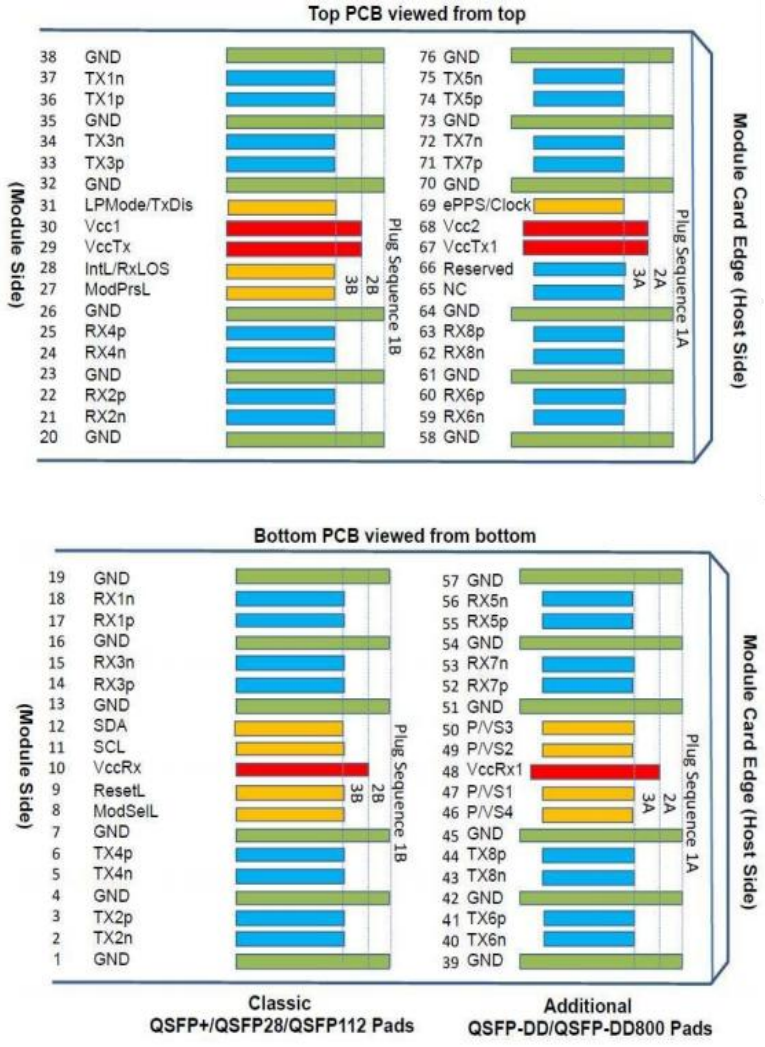

Figure 1 Pin definitions of the module high speed inputs/outputs

Pin Function Definitions

Table6-Pin Function Definitions

Pin	Logic	Symbol	Definition	Pin	Logic	Symbol	Definition
1		GND	Ground	39		GND	Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input	40	CML-I	Tx6n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-inverted Data Input	41	CML-I	Tx6p	Transmitter Non-inverted Data Input
4		GND	Ground	42		GND	Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input	43	CML-I	Tx8n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-inverted Data Input	44	CML-I	Tx8p	Transmitter Non-inverted Data Input
7		GND	Ground	45		GND	Ground
8	LVTTL-I	ModSelL	Module Select	46	LVCMOS/CML-I	P/VS4	Programmable/Module Vendor Specific 4
9	LVTTL-I	ResetL	Module Reset	47	LVCMOS/CML-I	P/VS1	Programmable/Module Vendor Specific 1
10		VccRx	+3 .3V Power Supply Receiver	48		VccRx1	3.3V Power Supply
11	LVCMOS-I/O	SCL	TWI serial interface clock	49	LVCMOS/CML-O	P/VS2	Programmable/Module Vendor Specific 2
12	LVCMOS-I/O	SDA	TWI serial interface data	50	LVCMOS/CML-O	P/VS3	Programmable/Module Vendor Specific 3
13		GND	Ground	51		GND	Ground
14	CML-O	Rx3p	Receiver Non-inverted Data Output	52	CML-O	Rx7p	Receiver Non-inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output	53	CML-O	Rx7n	Receiver Inverted Data Output
16		GND	Ground	54		GND	Ground
17	CML-O	Rx1p	Receiver Non-inverted Data Output	55	CML-O	Rx5p	Receiver Non-inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output	56	CML-O	Rx5n	Receiver Inverted Data Output
19		GND	Ground	57		GND	Ground
20		GND	Ground	58		GND	Ground
21	CML-O	Rx2n	Receiver Inverted Data Output	59	CML-O	Rx6n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-inverted Data Output	60	CML-O	Rx6p	Receiver Non-inverted Data Output
23		GND	Ground	61		GND	Ground

24	CML-O	Rx4n	Receiver Inverted Data Output	62	CML-O	Rx8n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-inverted Data Output	63	CML-O	Rx8p	Receiver Non-inverted Data Output
26		GND	Ground	64		GND	Ground
27	LVTTL-O	ModPrsL	Module Present	65		NC	Not connected
28	LVTTL-O	IntL/ RxLOS	Interrupt/optional RxLOS	66		Reserved	
29		VccTx	+3 .3V Power Supply Transmitter	67		VccTx1	3.3V Power Supply
30		Vcc1	+3 .3V Power Supply	68		Vcc2	3.3V Power Supply
31	LVTTL-I	LPMode/ TxDis	Low Power mode/optional TX Disable	69	LVCMOS-I	ePPS/Cloc k	1PPS PTP clock or reference clock input
32		GND	Ground	70		GND	Ground
33	CML-I	Tx3p	Transmitter Non-inverted Data Input	71	CML-I	Tx7p	Transmitter Non-inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input	72	CML-I	Tx7n	Transmitter Inverted Data Input
35		GND	Ground	73		GND	Ground
36	CML-I	Tx1p	Transmitter Non-inverted Data Input	74	CML-I	Tx5p	Transmitter Non-inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input	75	CML-I	Tx5n	Transmitter Inverted Data Input
38		GND	Ground	76		GND	Ground

Recommended QSFP-DD Host Board Schematic

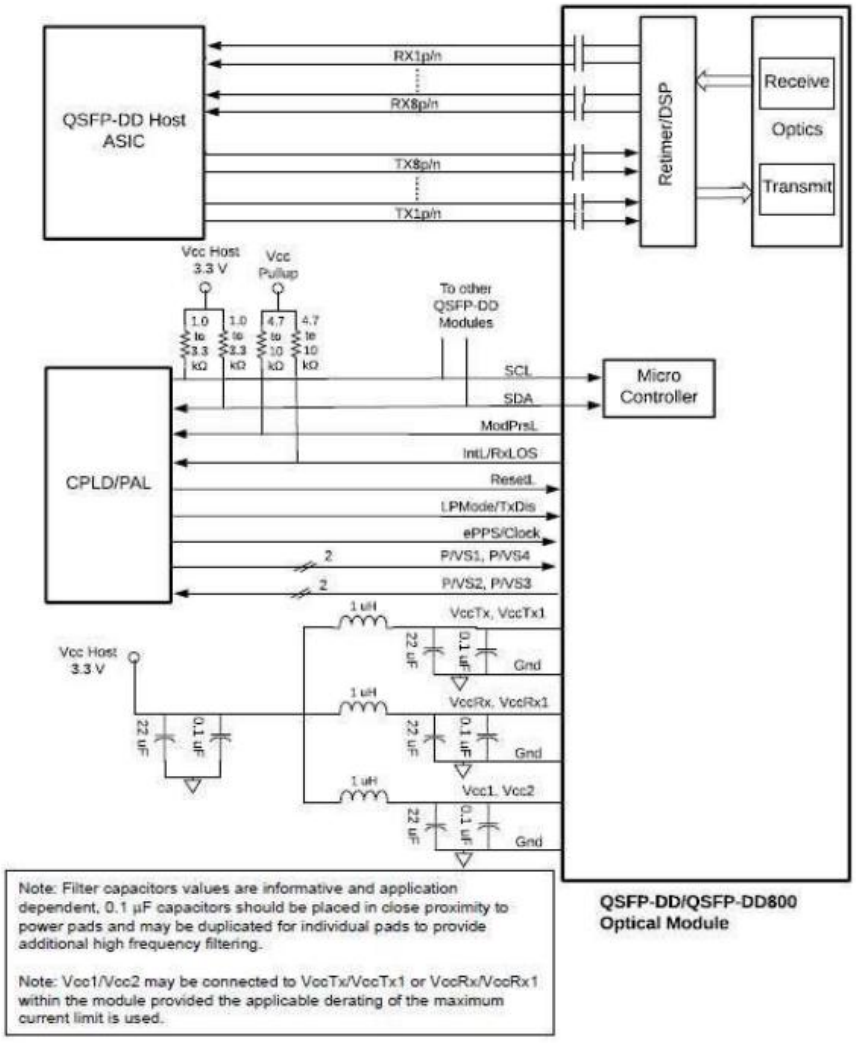

Figure 2 Recommended QSFP-DD/QSFP-DD800 Host Board Schematic

Digital Diagnostics

Parameter	Range	Accuracy.	Unit.	Calibration
Temperature	0 to 70	±3	°C	Internal
Voltage	0 to VCC	0.1	V	Internal
Tx Bias Current (Each Lane)	0 to 100	10%	mA	Internal
Tx Output Power (Each Lane)	-2.8 to +5.3	±3	dB	Internal
Rx Receive Power (Each Lane)	-9. 1 to +5.3	±3	dB	Internal

Dimensions of Transceiver

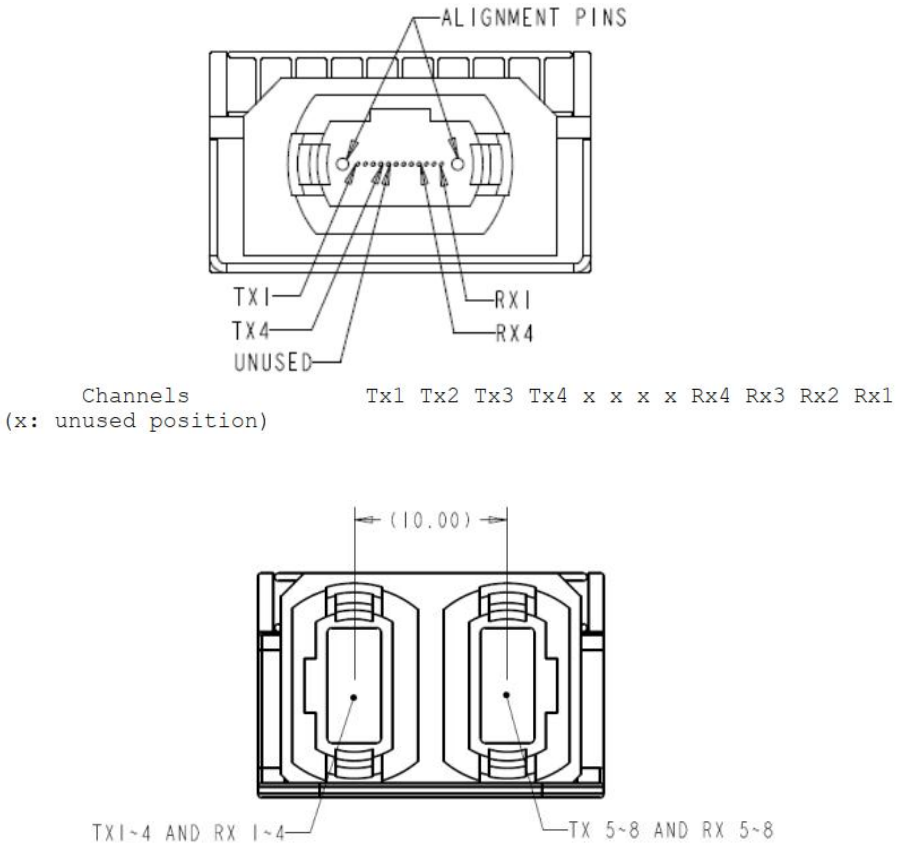

Figure 3 Dimensions of Transceiver

Further Information:

Web www.naddod.com

Email For order requirements: sales@naddod.com

For customer service: support@naddod.com

For technical support: tech@naddod.com

For cooperation: agency@naddod.com

For other informations: info@naddod.com

Disclaimer

1. We are committed to continuous product improvement and feature upgrades, and the contents contained in this manual are subject to change without notice.

2. Nothing herein should be construed as constituting an additional warranty.

3. NADDOD assumes no responsibility for the use or reliability of equipment or software not provided by NADDOD.