800Gb/s OSFP 2xFR4L 1310nm 6km Optical Transceiver

Features

- OSFP MSA 4.1 compliant
- 8x106.25Gb/s PAM4 electrical interface
- Maximum power consumption 16W@ Tcase = 70℃
- Dual Duplex LC connector
- 2x CWDM4 MUX/DEMUX design
- Up to 6km transmission on single mode fiber
- Operating case temperature: 0 ~70℃
- Single 3.3V power supply
- RoHS-6 compliant

Applications

- 2x400G Ethernet
- Data Center Applications
- Enterprise networking

Description

The OSFP-800G-2xFR4L Optical Transceiver is a high performance, cost effective module for optical data communication applications supporting 800G Ethernet. The OSFP-800G-2xFR4L is designed to operate in switch and router applications supporting OSFP MSA compliant traffic for up to 6km links. 850 Gigabit signal is carried over 2xCWDM4 lanes.

The OSFP-800G-2xFR4L can convert 8-channel 106.25Gb/s electrical data to 8-channel 106.25Gb/s optical signals. Similarly, it optically converts 8-channel 106.25Gb/s optical signals to 8-channel electrical data output on the receiver side. It has been designed to with stand the maximum range of external operating conditions including temperature, humidity and EMI. The module offers very high functionality and feature integration, accessible via a two-wire serial interface.

Absolute Maximum Ratings

Table1-Absolute Maximum Ratings

Parameter	Symbols	Min.	Max	Unit	Notes
Storage Temperature Range	TS	-40	85	°C	
Supply Voltage	VCC	-0.5	3.6	V	
Relative Humidity (non-condensing)	RH	5	85	%	1
Optical Input Power	PIN		4.5	dBm	

Note:

1: Non-condensing.

Recommended Operating Conditions

Table2-Recommended Operating Conditions

Parameter	Symbols	Min.	Typical	Max.	Unit	Notes
Operating Case Temperature	Tcase	0		70	ºC	
Power Supply Voltage	VCC	3.135	3.3	3.465	V	
Supply Current	ICC			5104	mA	Tcase =70℃
Module Power Dissipation	P			16	W	Tcase =70℃

Optical Electrical Characteristic

Table3-Optical Electrical Characteristic

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Wavelength Assignment	L0	1264.5	1271	1277.5	nm	
	L1	1284.5	1291	1297.5	nm	
	L2	1304.5	1311	1317.5	nm	
	L3	1324.5	1331	1337.5	nm	
Transmitter						
Optical Data Rate, each Lane		53.125 ± 100ppm			GBd	
Modulation Format		PAM4				
Total Average Launch Power				9.5	dBm	
Average Launch Power, each lane	P_{AVG}	-3.3		3.5	dBm	
Optical Modulation Amplitude (OMA), each lane	OMA	0.3		3.7	dBm	
Extinction Ratio	ER	3.5			dB	
Side-Mode Suppression Ratio	SMSR	30			dB	
Launch power in OMA minus TDECQ, each lane, for ER≥4.5dB		-1.7			dBm	
Launch power in OMA minus TDECQ, each lane, for ER＜4.5dB		-1.6				
Transmitter and Dispersion Eye Closure for PAM4, each Lane	TDECQ	3.4			dB	
Difference in Launch Power				4	dB	

between any Two Lanes (OMAouter)						
Optical Return Loss Tolerance				17.1	dB	
Transmitter Reflectance				-26	dB	
Average Launch Power of OFF Transmitter, each Lane				-20	dBm	
Electrical Data Rate, each lane			53.125 ± 100ppm		GBd	
Differential pk-pk input Voltage tolerance	Vpp	600			mV	
DC Common Mode Voltage	Vcm	-350		2850	mV	Note1
Differential Termination Resistance Mismatch		-10		10	%	
Effective return loss				8.5	dB	
Differential to Common Mode Input Return Loss			IEEE 802.3ck Equation (120G-2)		dB	
Module Stressed Input Test			IEEE 802.3ck Equation (120G-2)			Note2
Receiver						
Optical Data Rate, each Lane			53.125±100ppm		GBd	
Modulation Format			PAM4			
Damage Threshold, each lane		4.5			dBm	
Average receiver power, each lane		-7.3		3.5	dBm	

Receiver power, each lane (OMA)				3.7	dBm	
Difference in Receiver Power between any Two Lanes (OMA)				4.1	dB	
Receiver Sensitivity (OMAouter) , each lane				max(-4.6, SECQ-6)	dBm	
Stressed receiver sensitivity (OMAouter), each laned (max)				-1.9	dBm	
Receiver reflectance				-26	dB	
Electrical Data Rate, each lane			53.125±100ppm		GBd	
Differential Termination Resistance Mismatch		-10		10	%	
Differential output Voltage pk-pk	Vpp			600	mV	
DC Common Mode Voltage	Vcm	-350		2850	mV	Note1
Effective return loss	ERL	8.5			dB	
Transition time		8.5			ps	
Common mode to differential return loss			IEEE 802.3ck Equation (120G-1)		dB	

Notes:

1: DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

2: BER specified in IEEE 802.3ck 120G.1.1.

Digital Diagnostic Functions and Control and Status I/O Timing Characteristics

Table4-Digital Diagnostic Functions and Control and Status I/O Timing Characteristics

Parameter	Symbols	Min.	Typical	Max.	Unit	Notes
Temperature monitor absolute error	DMI_Temp	–3		3		Note1
Supply voltage monitor absolute error	DMI_Vcc	–3%		3%		Note2
Bias current monitor absolute error	DMI_Ibias	–10%		10%		
Laser power monitor absolute error	DMI_Tx	–3		3		
RX power monitor absolute error	DMI_Rx	–3		3		

Notes:

1: Temperature here is depending on module case around Max power dissipation. Temperature monitor is done over operating temperature.

2: Supply voltage monitor is done over operating voltage.

Control and Status I/O Timing Characteristics

Table5-Control and Status I/O Timing Characteristics

Parameter	Symbols	Min.	Typical	Max.	Unit	Notes
MgmtInitDuration	Max MgmtInit Duration			2000	ms	Note1
ResetL Assert Time	t_reset_init	10			μm	Note2
IntL Assert Time	ton_IntL			200	ms	Note3
IntL Deassert Time	toff_IntL			500	μm	Note4
Rx LOS Assert Time	ton_los			100	ms	Note5
Tx Fault Assert Time	ton_Txfault			200	ms	Note6
Flag Assert Time	ton_flag			200	ms	Note7
Mask Assert Time	ton_mask			100	ms	Note8
Mask Deassert Time	toff_mask			100	ms	Note9

Notes:

1:Time from power on, hot plug or rising edge of reset until completion of the MgmtInit State.

2: Minimum pulse time on the ResetL signal to initiate a module reset.

3: Time from occurrence of condition triggering IntL until Vout:IntL=Vol.

4: Time from clear on read operation of associated flag until Vout:IntL=Voh.This includes deassert times for Rx LOS, Tx Fault and other flag bits.

5: Time from Rx LOS state to Rx LOS bit set (value = 1b) and IntL asserted.

6: Time from Tx Fault state to Tx Fault bit set (value=1b) and IntL asserted.

Surge Current Requirements

Table6-Surge Current Requirements

Parameter	Symbols	Min.	Typical	Max.	Unit	Notes
Module power supply voltage including ripple, droop and noise below 100 kHz	Vcc_Module	3.135	3.3	3.465	V	
Host power supply voltage including ripple, droop and noise below 100 kHz	Vcc_Host	3.135	3.3	3.465	V	
Module power supply noise tolerance 10 Hz – 10 MHz (peak–to–peak) Voltage drop across mated connector(Vcc_Host – Vcc_Module)	Vcc_drop			66	mV	
Total current for Vcc pins	Icc_module			10	A	Note1
Host RMS noise output 10 Hz–10 MHz	e N_Host			25	mV	
Module RMS noise output 10 Hz – 10 MHz	e N_Mod			15	m	
Module inrush – instantaneous peak duration	T_ip			50	us	
Module inrush – initialization time	T_init			500	ms	
Inrush and Discharge Current	I_didt			100	mA/us	Note2
High power mode to Low power mode transition time from assertion of M_LPWn or M_RSTn or ForceLowPwr	T_hplp			200	us	

High Power Mode Power Class 8 module						
Power Consumption	P_8			16	W	
Instantaneous peak current	Icc_ip_8			6400	mA	
Sustained peak current	Icc_sp_8			5328	mA	
Steady state current	Icc_8			5104	mA	Note3

Notes:

1:Utilization of the maximum OSFP power rating requires thermal design and validation at the system level to ensure the maximum connector temperature is not exceeded. A recommended design practice is to heatsink the host board power pin pads with multiple vias to a thick copper power plane for conductive cooling.

2: The specified Inrush and Discharge Current (I_didt) limit shall not be exceeded for all power transient events. This includes hot-plug, hot-unplug, power-up, power-down, initialization, low-power to high power and high-power tolow-power.

3: Steady state current must not allow power consumption to exceed the specified maximum power for the selected power class.

Pin Description

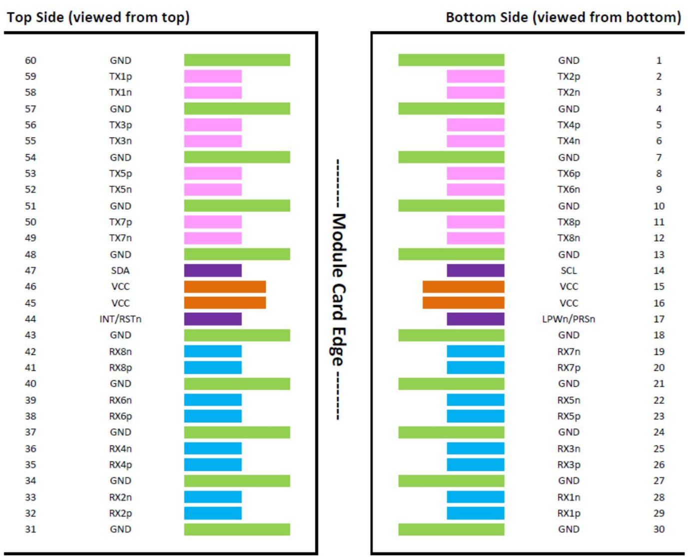

Figure 1 Pin out definitions of OSFP module inputs/outputs

Pin Function Definitions

Table7-Pin Function Definitions

Pin	Symbol	Description	Logic	Notes
1	GND	Ground		Note1
2	TX2p	Transmitter Data Non-Inverted	CML-I	
3	TX2n	Transmitter Data Inverted	CML-I	
4	GND	Ground		Note1
5	TX4p	Transmitter Data Non-Inverted	CML-I	
6	TX4n	Transmitter Data Inverted	CML-I	
7	GND	Ground		Note1
8	TX6p	Transmitter Data Non-Inverted	CML-I	
9	TX6n	Transmitter Data Inverted	CML-I	
10	GND	Ground		Note1
11	TX8p	Transmitter Data Non-Inverted	CML-I	
12	TX8n	Transmitter Data Inverted	CML-I	
13	GND	Ground		Note1
14	SCL	2-wire Serial interface clock	LVCMOS-I/O	Note2
15	VCC	+3.3V Power		
16	VCC	+3.3V Power		
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	Note3
18	GND	Ground		Note1
19	RX7n	Receiver Data Inverted	CML-O	

20	RX7p	Receiver Data Non–Inverted	CML–O	
21	GND	Ground		Note1
22	RX5n	Receiver Data Inverted	CML–O	
23	RX5p	Receiver Data Non–Inverted	CML–O	
24	GND	Ground		Note1
25	RX3n	Receiver Data Inverted	CML–O	
26	RX3p	Receiver Data Non–Inverted	CML–O	
27	GND	Ground		Note1
28	RX1n	Receiver Data Inverted	CML–O	
29	RX1p	Receiver Data Non–Inverted	CML–O	
30	GND	Ground		Note1
31	GND	Ground		Note1
32	RX2p	Receiver Data Non–Inverted	CML–O	
33	RX2n	Receiver Data Inverted	CML–O	
34	GND	Ground		Note1
35	RX4p	Receiver Data Non–Inverted	CML–O	
36	RX4n	Receiver Data Inverted	CML–O	
37	GND	Ground		Note1
38	RX6p	Receiver Data Non–Inverted	CML–O	
39	RX6n	Receiver Data Inverted	CML–O	
40	GND	Ground		Note1
41	RX8p	Receiver Data Non–Inverted	CML–O	

42	RX8n	Receiver Data Inverted	CML–O	
43	GND	Ground		Note1
44	INT/RSTn	Module Interrupt / Module Reset	Multi– Level	Note4
45	VCC	+3.3V Power		
46	VCC	+3.3V Power		
47	SDA	2–wire Serial interface data	LVCM OS–I/O	Note2
48	GND	Ground		Note1
49	TX7n	Transmitter Data Inverted	CML–I	
50	TX7p	Transmitter Data Non–Inverted	CML–I	
51	GND	Ground		Note1
52	TX5n	Transmitter Data Inverted	CML–I	
53	TX5p	Transmitter Data Non–Inverted	CML–I	
54	GND	Ground		Note1
55	TX3n	Transmitter Data Inverted	CML–I	
56	TX3p	Transmitter Data Non–Inverted	CML–I	
57	GND	Ground		Note1
58	TX1n	Transmitter Data Inverted	CML–I	
59	TX1p	Transmitter Data Non–Inverted	CML–I	
60	GND	Ground		Note1

Notes:

1:OSFP uses common ground (GND) for all signals and supply (power). All are common within the OSFP module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal–common ground plane.

2: SCL and SDA are a 2-wire serial interface between the host and module using the I2C or I3C protocols. SCL is defined as the serial interface clock signal and SDA as the serial interface data signal. Both signals are open-drain and require pull-up resistors to +3.3V on the host. The pull-up resistor value shall be 1k ohms to 4.7k ohms depending on capacitive load.

3: LPWn/PRSn is a dual function signal that allows the host to signal Low Power mode and the module to indicate Module Present. The circuit shown in Figure 2 enables multi-level signaling to provide direct signal control in both directions. Low Power mode is an active-low signal on the host which gets converted to an active-low signal on the module. Module Present is controlled by a pull-down resistor on the module which gets converted to an active-low logic signal on the host.

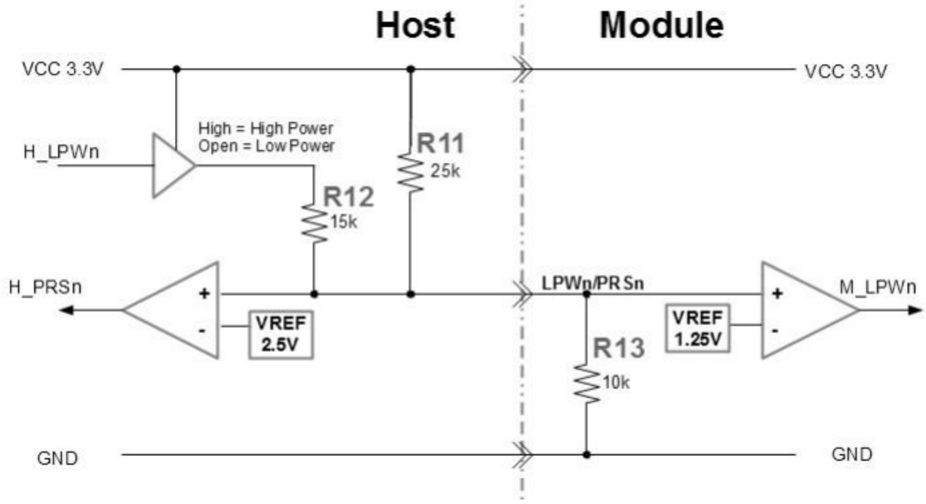

Figure 2 LPWn/PRSn circuit

4: INT/RSTn is a dual function signal that allows the module to raise an interrupt to the host and also allows the host to reset the module. The circuit shown in Figure 3 enables multi-level signaling to provide direct signal control in both directions. Reset is an active-low signal on the host which is translated to an active-low signal on the module. Interrupt is an active-high signal on the module which gets translated to an active-low signal on the host.

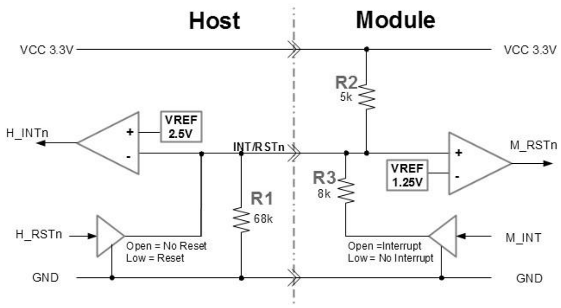

Figure 3 INT/RSTn circuit

Digital Diagnostic of Transceiver

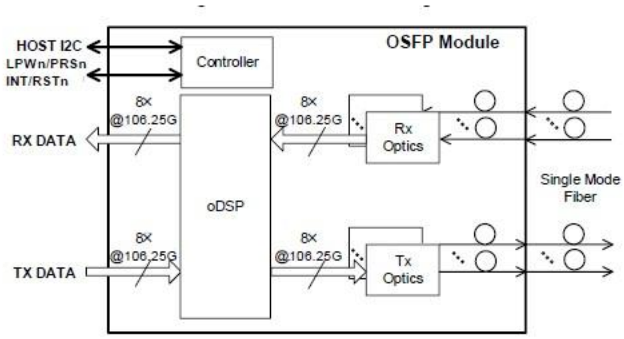

Figure4 Block Diagram of Transceiver

＜Transmitter Section＞: The OSFP-800G-2xFR4L converts 8-channel 106.25Gb/s electrical data to 8-channel 2xCWDM4 106.25Gb/s optical signals for 850Gb/s optical transmission.

＜Receiver Section＞: Similarly, it optically converts 8-channel 2xCWDM4 106.25Gb/s optical signals to 8-channel electrical data output on the receiver side.

Recommended Interface Circuit

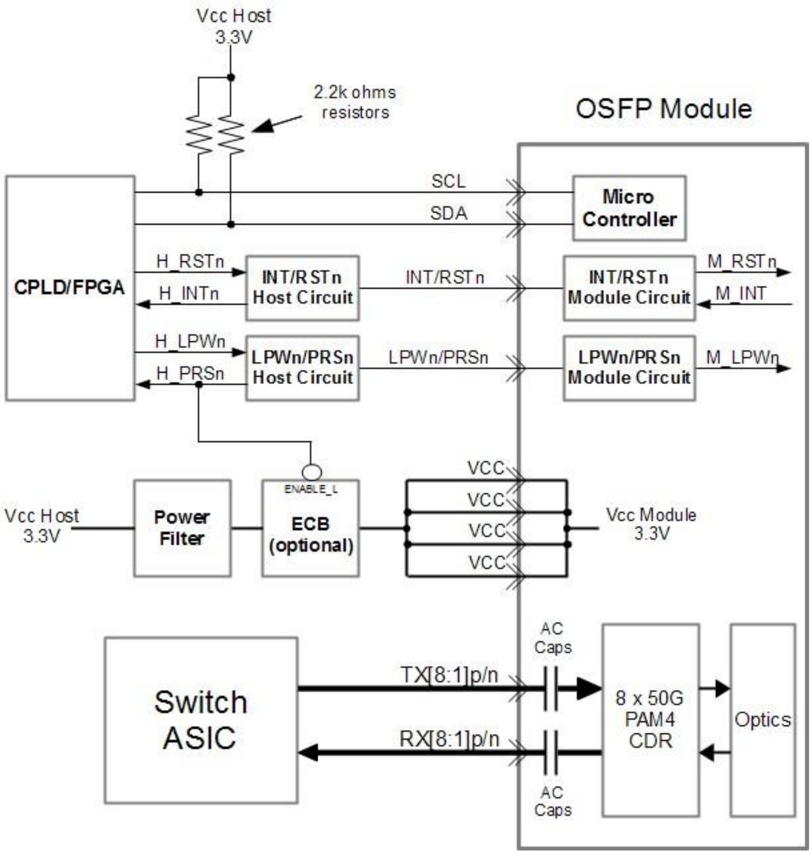

Figure5 Host board and Module block diagram

Dimensions

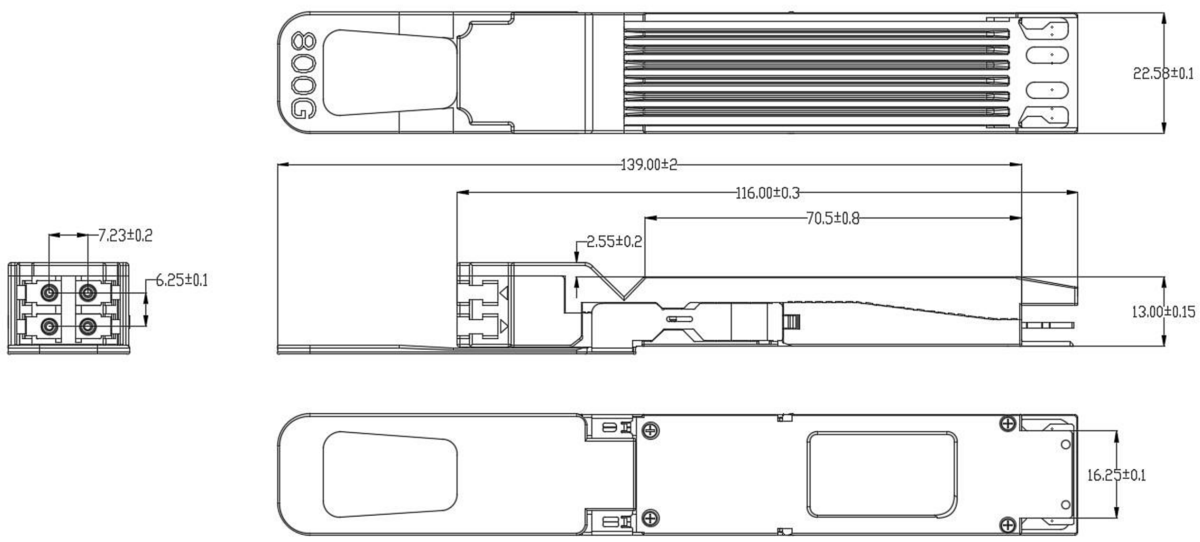

Figure6 Dimensions of Transceiver

Digital Diagnostic Memory Map

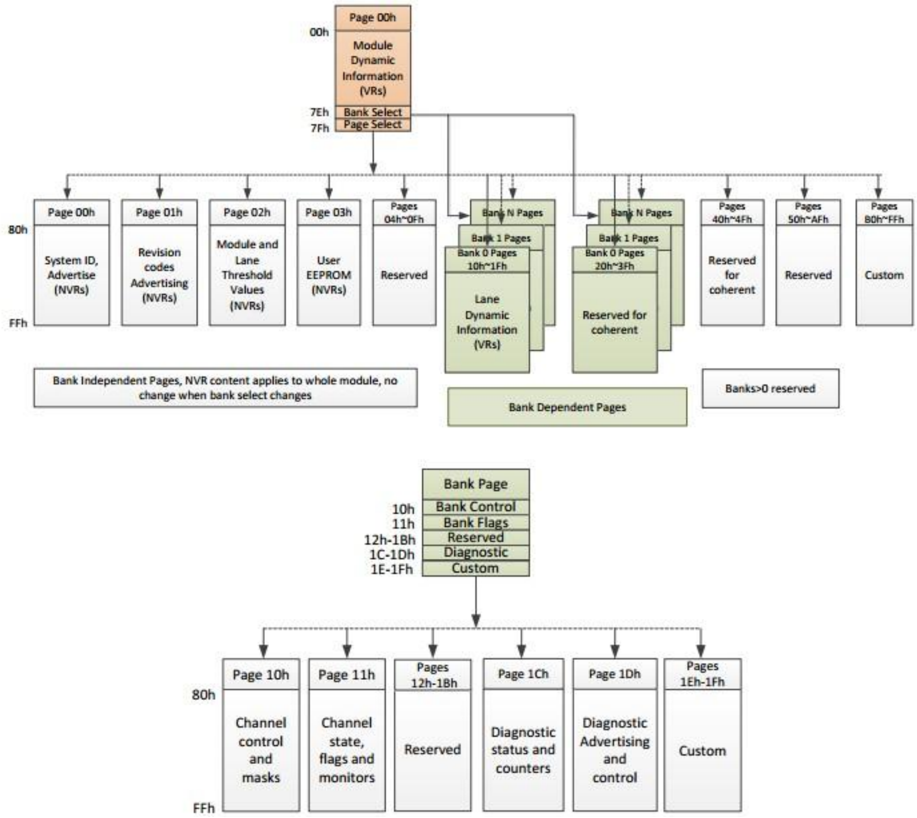

Figure7 Digital Diagnostic Memory Map

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