1.6Tb/s Twin-port XDR OSFP 2xDR4 1310nm 500m Optical Transceiver

Features

- InfiniBand and Ethernet
- 8x212Gb/s PAM4 electrical interface
- OSFP MSA package with 2*MPO-12
- Up to 500m transmission on single mode fiber
- Silicon photonics-based transmitter with 1310nm DFB lasers and PIN receiver
- Single 3.3V power supply
- Electrically hot-pluggable
- Power consumption < 25W
- Case temperature range of 0 to 70°C
- 2-wire interface for integrated digital diagnostic monitoring
- Very low EMI and excellent ESD protection

Applications

- AI cluster
- 1.6T Ethernet
- DCI

Compliance

- OSFP MSA Rev5.0
- IEEE 802.3dj_D2.0
- CMIS Rev5.2
- RoHS compliance

Description

The OSFP-1.6T-2xDR4H is a cost-effective module with high performance, which is optimized for AI Datacenter, supporting data-rate of 8x212Gb/s PAM4 Optical interface and 8x212Gb/s PAM4 Electrical interface. Its transmission distance is up to 500m on single mode fibers.

The OSFP-1.6T-2xDR4H can convert 8x212Gb/s electrical data to 8x212Gb/s optical signals. Similarly, it converts 8x212Gb/s optical signals to 8x212Gb/s output electrical data on the receiver side. It has been designed to withstand the maximum range of external operating conditions including temperature, humidity and EMI. The module offers very high functionality and feature integration, accessible via a two-wire serial interface.

Absolute Maximum Ratings

Table1-Absolute Maximum Ratings

Parameter	Symbols	Min.	Typical	Max.	Unit	Notes
Storage Temperature	TS	-40		+85	ºC	
Operating Relative Humidity (non-condensing)	RH	5		85	%	
Supply Voltage	VCC	-0.5	3.3	3.6	V	
Receiver Damage Threshold, each lane		5			dBm	

Recommended Operating Conditions

Table2-Recommended Operating Conditions

Parameter	Symbols	Min.	Typical	Max.	Unit	Notes
Case Temperature	Top	0		+70	℃	
Supply Voltage	VCC	3.135	3.3	3.465	V	
Supply Current	ICC			7974	mA	Tcase =70℃
Module Power Dissipation	P			25	W	Tcase =70℃

Operating Characteristic-Optical，Electrical

Table3-Optical，Electrical Characteristic

Parameter	Symbol	Min	Typical	Max	Units	Notes
Transmitter						
Optical Data Rate, each Lane			106.25±100ppm		GBd	
Modulation Format			PAM4			
Line wavelengths	λ	1304.5	1311	1317.5	nm	
Average Launch Power, each lane	PAVG	-3.3		4	dBm	
Optical Modulation Amplitude (OMA), each lane	OMA	-0.3		4.2	dBm	
Extinction Ratio	ER	3.5			dB	
Side-Mode Suppression Ratio	SMSR	30			dB	
Launch power in OMA minus TDECQ, each lane		-1.2			dB	
Transmitter and Dispersion Eye Closure for PAM4, each Lane	TDECQ			3.4	dB	
Optical Return Loss Tolerance				21.4	dB	
Transmitter Reflectance				-26	dB	
Average Launch Power of OFF Transmitter, each Lane				-15	dBm	
Electrical Data Rate, each lane			106.25±100ppm		GBd	
Differential pk-pk input Voltage	Vpp			1	V	
DC Common Mode Voltage	Vcm	0		1	V	
Differential Termination Resistance Mismatch	Rdm	-10		10	%	
Receiver						
Optical Data Rate, each Lane			106.25±100ppm		GBd	
Modulation Format			PAM4			
Line wavelengths	λ	1304.5	1311	1317.5	nm	
Average receiver power, each lane		-6.3		4	dBm	
Receiver power, each lane (OMA)				4.2	dBm	

Receiver Sensitivity (OMAouter), each lane				max(-3.4, TECQ-4.3)	dBm	Note 1
Stressed receiver sensitivity (OMAouter), each laned (max)				-0.9	dBm	
Receiver reflectance				-26	dB	
LOS Assert	LOS_A	-15			dBm	
LOS Deassert	LOS_D			-9	dBm	
LOS Hysteresis		0.5		3	dB	
Electrical Data Rate, each lane			106.25±100ppm		GBd	
Differential Termination Resistance Mismatch		-10		10	%	
Differential output Voltage pk-pk	Vpp			1	V	
DC Common Mode Voltage	Vcm	0		1	V	

Note:

[1] Receiver sensitivity (OMAouter), each lane (max) is informative and is defined for a transmitter with TECQ of 0.9 dB. Receiver sensitivity (OMAouter), each lane:for TECQ＜0.9dB,max=-3.4(dBm).For 0.9dB≤TECQ≤SECQ,max=TECQ-4.3(dBm).

Digital Diagnostic Functions

Table4-Digital Diagnostic Functions

Parameter	Symbol	Min	Typical	Max	Units	Notes
Temperature monitor absolute error	DMI_Temp	-3		3	℃	Note1
Supply voltage monitor absolute error	DMI_Vcc	-3%		3%	V	Note2
Bias current monitor absolute error	DMI_Ibias	-10%		10%	mA	
Laser power monitor absolute error	DMI_Tx	-3		3	dB	
RX power monitor absolute error	DMI_Rx	-3		3	dB	

Notes:

[1] Temperature here is depending on module case around Max power dissipation. Temperature monitor is done over operating temperature.

[2] Supply voltage monitor is done over operating voltage.

Control and Status I/O Timing Characteristics

Table5-Control and Status I/O Timing Characteristics

Parameter	Symbol	Min	Typical	Max	Units	Notes
MgmtInitDuration	Max MgmtInit Duration			2000	ms	Note1

ResetL Assert Time	t_reset_init	10			μs	Note2
IntL Assert Time	ton_IntL			200	ms	Note3
IntL Deassert Time	toff_IntL			500	μs	Note4
Rx LOS Assert Time	ton_los			100	ms	Note5

Notes:

[1] Time from power on, hot plug or rising edge of reset until completion of the MgmtInit State.

[2] Minimum pulse time on the ResetL signal to initiate a module reset.

[3] Time from occurrence of condition triggering IntL until Vout:IntL=Vol.

[4] Time from clear on read operation of associated flag until Vout:IntL=Voh.This includes deassert times for Rx LOS, Tx Fault and other flag bits.

[5] Time from Rx LOS state to Rx LOS bit set (value = 1b) and IntL asserted.

[6] Time from occurrence of condition triggering flag to associated flag bit set (value=1b) and IntL asserted.

[7] Time from mask bit set (value=1b) until associated IntL assertion is inhibited.

[8] Time from mask bit cleared (value=0b) until associated IntL operation resumes.

Table6-Surge Current Requirements

Parameter	Symbol	Min	Typical	Max	Units	Notes
Module power supply voltage including ripple,droop and noise below 100 kHz	Vcc_Module	3.135	3.3	3.465	V	
Host power supply voltage including ripple, droop and noise below 100 kHz	Vcc_Host	3.135	3.3	3.465	V	
Module power supply noise tolerance 10 Hz - 10 MHz (peak-to-peak) Voltage drop across mated connector(Vcc_Host minus Vcc_Module)	Vcc_drop			66	mV	
Total current for Vcc pins	Icc_module			10	A	Note1
Host RMS noise output 10 Hz-10 MHz	e N_Host			25	mV	
Module RMS noise output 10 Hz - 10 MHz	e N_Mod			15	mV	
Module inrush - instantaneous peak duration	T_ip			50	μs	
Module inrush - initialization time	T_init			500	ms	
Inrush and Discharge Current	I_didt			100	mA/μs	Note2
High power mode to Low power mode transition time from assertion of M_LPWn or M_RSTn or ForceLowPwr	T_hplp			200	μs	

Notes:

[1] Utilization of the maximum OSFP power rating requires thermal design and validation at the system level to ensure the maximum connector temperature is not exceeded. A recommended design practice is to heatsink the host board power pin pads with multiple vias to a thick copper power plane for conductive cooling.

[2] The specified Inrush and Discharge Current (I_didt) limit shall not be exceeded for all power transient events. This includes hot-plug, hot-unplug, power-up, power-down, initialization, low-power to high power and high-power to low-power.

Pin Description

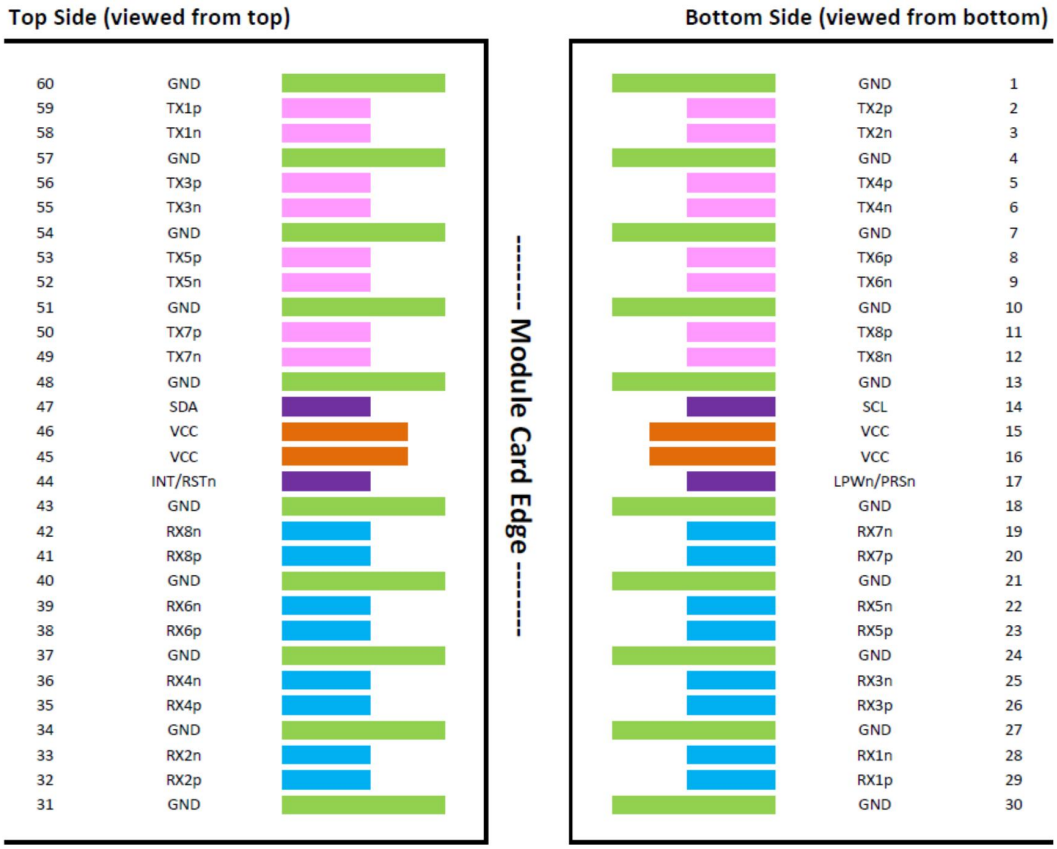

Figure1 OSFP module pinout

Pin Function Definitions

Table7-Pin Function Definitions

Pin	Symbol	Description	Logic	Notes
1	GND	Ground		1
2	Tx2p	Transmitter Data Non-Inverted	CML-I	3
3	Tx2n	Transmitter Data Inverted	CML-I	3
4	GND	Ground		1
5	Tx4p	Transmitter Data Non-Inverted	CML-I	3
6	Tx4n	Transmitter Data Inverted	CML-I	3
7	GND	Ground		1
8	TX6p	Transmitter Data Non-Inverted	CML-I	3
9	Tx6n	Transmitter Data Inverted	CML-I	3
10	GND	Ground		1

11	Tx8p	Transmitter Data Non-Inverted	CML-I	3
12	Tx8n	Transmitter Data Inverted	CML-I	3
13	GND	Ground		1
14	SCL	2-wire serial interface clock	LVCMOS-I/O	3
15	VCC	+3.3V Power		2
16	VCC	+3.3V Power		2
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	3
18	GND	Ground		1
19	Rx7n	Receiver Data Inverted	CML-O	3
20	Rx7p	Receiver Data Non-Inverted	CML-O	3
21	GND	Ground		1
22	Rx5n	Receiver Data Inverted	CML-O	3
23	Rx5p	Receiver Data Non-Inverted	CML-O	3
24	GND	Ground		1
25	Rx3n	Receiver Data Inverted	CML-O	3
26	Rx3p	Receiver Data Non-Inverted	CML-O	3
27	GND	Ground		1
28	Rx1n	Receiver Data Inverted	CML-O	3
29	Rx1p	Receiver Data Non-Inverted	CML-O	3
30	GND	Ground		1
31	GND	Ground		1
32	Rx2p	Receiver Data Non-Inverted	CML-O	3
33	Rx2n	Receiver Data Inverted	CML-O	3
34	GND	Ground		1
35	Rx4p	Receiver Data Non-Inverted	CML-O	3
36	Rx4n	Receiver Data Inverted	CML-O	3
37	GND	Ground		1
38	Rx6p	Receiver Data Non-Inverted	CML-O	3
39	Rx6n	Receiver Data Inverted	CML-O	3
40	GND	Ground		1
41	Rx8p	Receiver Data Non-Inverted	CML-O	3
42	Rx8n	Receiver Data Inverted	CML-O	3
43	GND	Ground		1
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	3
45	VCC	+3.3V Power		2
46	VCC	+3.3V Power		2
47	SDA	2-wire Serial interface data	LVCMOS-I/O	3
48	GND	Ground		1
49	Tx7n	Transmitter Data Inverted	CML-I	3

50	Tx7p	Transmitter Data Non-Inverted	CML-I	3
51	GND	Ground		1
52	Tx5n	Transmitter Data Inverted	CML-I	3
53	Tx5p	Transmitter Data Non-Inverted	CML-I	3
54	GND	Ground		1
55	Tx3n	Transmitter Data Inverted	CML-I	3
56	Tx3p	Transmitter Data Non-Inverted	CML-I	3
57	GND	Ground		1
58	Tx1n	Transmitter Data Inverted	CML-I	3
59	Tx1p	Transmitter Data Non-Inverted	CML-I	3
60	GND	Ground		1

Notes:

[1] OSFP uses common ground (GND) for all signals and supply (power). All are common within the OSFP module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

[2] SCL and SDA are a 2-wire serial interface between the host and module using the I2C or I3C protocols. SCL is defined as the serial interface clock signal and SDA as the serial interface data signal. Both signals are open-drain and require pull-up resistors to +3.3V on the host. The pull-up resistor value shall be 1k ohms to 4.7k ohms depending on capacitive load.

[3] LPWn/PRSn is a dual function signal that allows the host to signal Low Power mode and the module to indicate Module Present. The circuit shown in Figure 2 enables multi-level signaling to provide direct signal control in both directions. Low Power mode is an active-low signal on the host which gets converted to an active-low signal on the module. Module Present is controlled by a pull-down resistor on the module which gets converted to an active-low logic signal on the host.

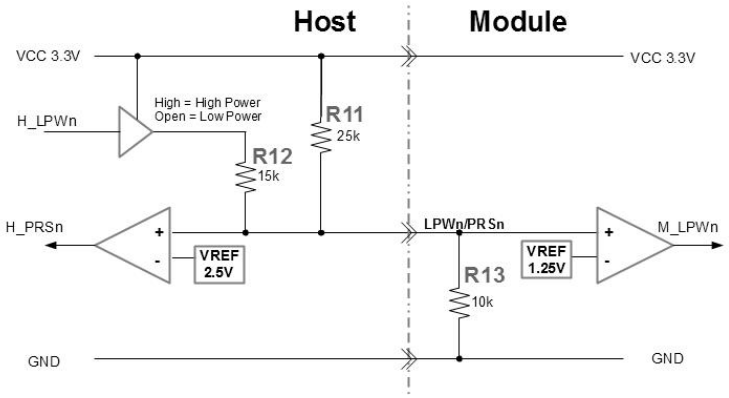

Figure2 INT/RSTn circuit

[4] INT/RSTn is a dual function signal that allows the module to raise an interrupt to the host and also allows the host to reset the module. The circuit shown in Figure 3 enables multi-level signaling to provide direct signal control in both directions. Reset is an active-low signal on the host which is translated to an active-low signal on the module. Interrupt is an active-high signal on the module which gets translated to an active-low signal on the host.

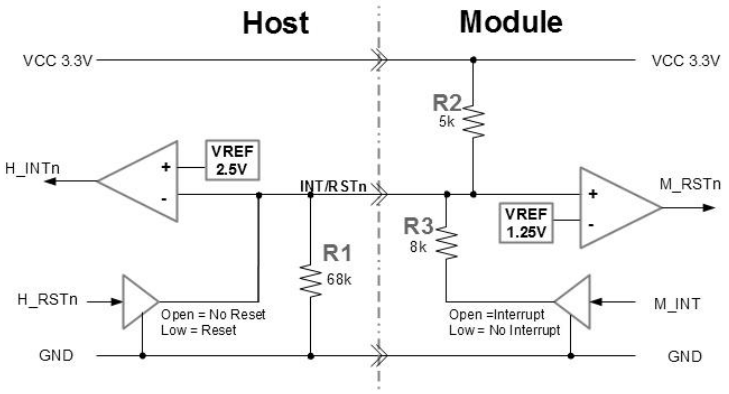

Figure3 Block Diagram of Transceiver

Block Diagram of Transceiver

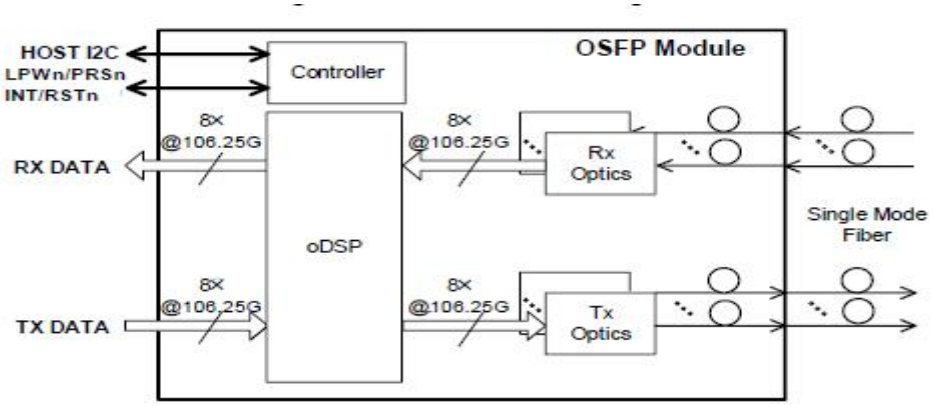

Figure 4 Block Diagram of Transceiver

<Transmitter Section>: The OSFP-1.6T-2xDR4H converts 8-channel 106.25Gbd electrical data to 8-channel 1311nm 106.25Gbd optical signals for 1.6Tbps optical transmission.

<Receiver Section>: Similarly, it optically converts 8-channel 1311nm 106.25Gbd optical signals to 8-channel electrical data output on the receiver side.

Dimensions of Transceiver

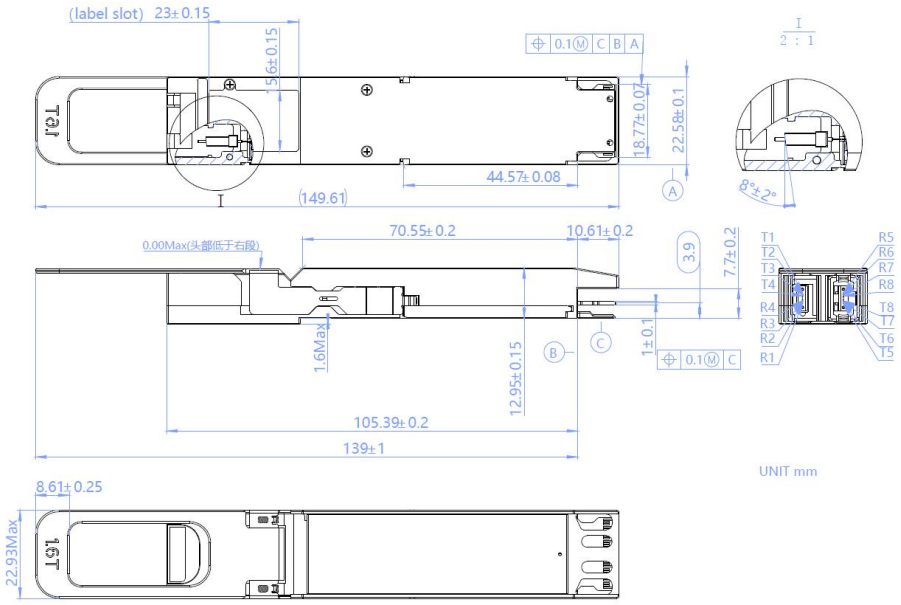

Figure5 Dimensions of Transceiver

Digital Diagnostic Memory Map

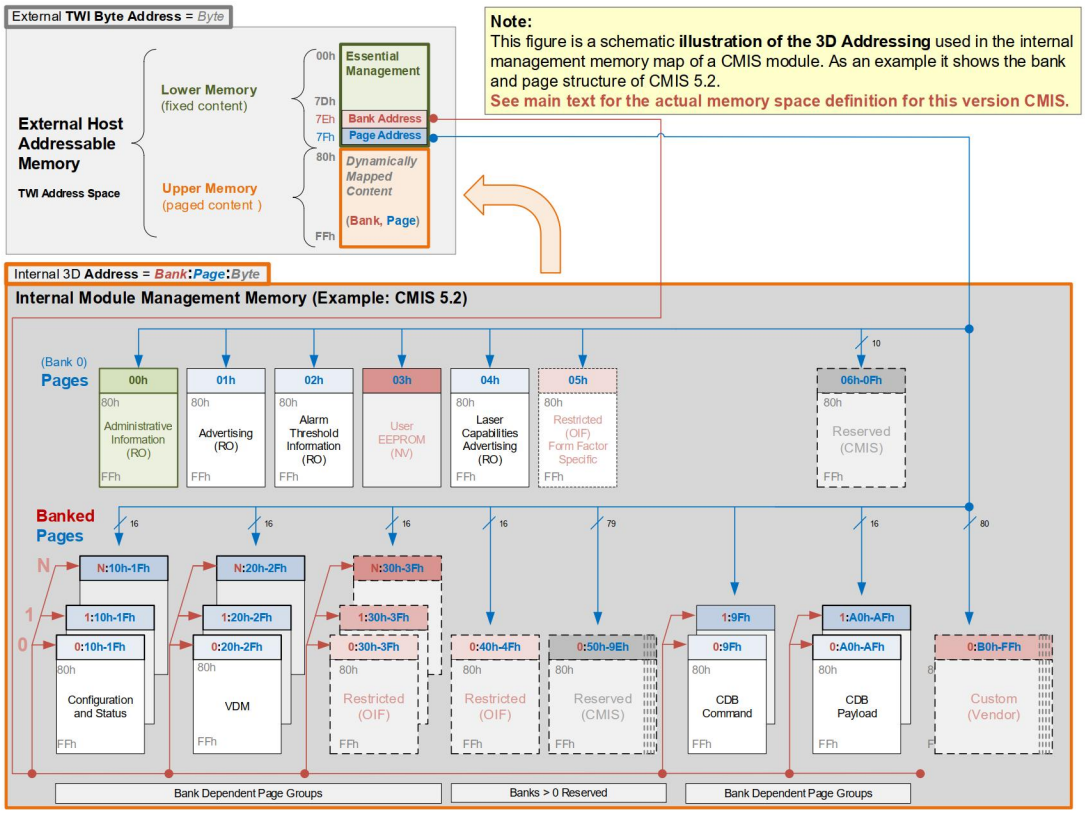

Figure6 Digital Diagnostic Memory Map

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