800G Twin-port NDR OSFP 2xDR4 100m Optical Transceiver

Features

- Supports 850Gbps
- Single 3.3V Power Supply
- Up to 100m over SMF with KP4 FEC supported at the Host side
- 8x106.25Gbps (PAM4) electrical interface
- Closed Finned-top/IHS OSFP
- SMF Dual MPO-12 APC connector
- Power dissipation < 16W
- Case temperature range: 0°C to 70°C
- Safety Certification: TUV/UL/FDA
- RoHS Compliant

Applications

- Used in 800G OSFP switches
- 800G Ethernet

Description

OSFP-800G-2xDR4S transceiver module is designed for use in use in 800 Gigabit links over 100m single mode fiber. The module includes eight parallel channels with a central wavelength of 1310nm, and the operating rate of each channel is 106.25Gbps. These 8-channel PAM4 parallel optical signals can be converted into 8-channel PAM4 electrical output signals; and there are 8 independent electrical input/output channels, which can convert PAM4 electrical input data into 8-channel PAM4 parallel optical signal. The electrical interface of the module is compliant with the 800GAUI-8 interface as defined by IEEE 802.3ck, and compliant with OSFP MSA.

Absolute Maximum Specifications

Absolute maximum ratings are those beyond which damage to the device may occur.

Prolonged operation between the operational specifications and absolute maximum ratings is not intended and may cause permanent device degradation.

Table1-Absolute Maximum Specifications

Parameter	Min.	Typical	Max.	Unit	Note
Storage Temperature	-40		+85	ºC	
Supply voltage	-0.5	3.3	3.6	V	
Relative Humidity (non- condensing)	5		85	%	
Data input voltage – single ended	-0.5		Vcc+0.5	V	
Data input voltage – differential			0.8	V	1
Operating Case Temperature	0		70	ºC	

Notes:

[1] This is the maximum voltage that can be applied across the differential inputs without damaging the input circuitry. The damage threshold of the module input shall be at least 1600mV peak to peak differential.

Recommended Operating Conditions

For operations beyond the recommended operating conditions, optical and electrical characteristics are not defined, reliability is not implied, and such operations for a long time may damage the module.

Table2-Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max.	Units	Note
Operating Case Temperature	Top	0		70	℃	
Power Supply Voltage	Vcc	3.135	3.3	3.465	V	
Total Power Consumption	Pc			16	W	
Electrical signal rate per channel (PAM encoded)			106.25		Gbps	1
Optical signal rate per channel (PAM encoded)			106.25		Gbps	2
Power supply noise				50	mVpp	3
Receiver differential data output load		100			Ohm	
Fiber length (9μm SMF)				100	m	4

Notes:

[1] 800G-DR8 operation with Host generated FEC. The transmitter must receive pre-coded FEC signals from the host ASIC.
[2] .800G operation with Host generated FEC. The transmitter must receive pre-coded FEC signals from the host ASIC.
[3] Power Supply Noise is defined as the peak-to-peak noise amplitude over the frequency range at the host supply side of the recommended power supply filter with the module and recommended filter in place. Voltage levels including peak-to-peak noise are limited to the recommended operating range of the associated power supply.
[4] The maximum link distance is based on an allocation of 3dB of attenuation and 3dB total connection and splice loss. The loss of a single connection shall not exceed 0.5dB.

General Electrical Characteristics

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

Table3-General Electrical Characteristics

Parameter	Min.	Typical	Max.	Unit	Note
Transceiver power consumption			16	W	
Transceiver power supply current, total			4394	mA	
AC coupling capacitors (internal)		0.1		uF	

Reference Points

Test Point	Description
TP0 to TP5	The channel including the transmitter and receiver differential controlled impedance printed circuit board insertion loss and the cable assembly insertion loss.
TP1 to TP4	All cable assembly measurements are made between TP1 and TP4.
TP0 to TP2 TP3 to TP5	A mated connector pair has been included in both the transmitter and receiver specifications defined in 802.3ck 162.9.3 and 162.9.4. The recommended maximum insertion loss from TP0 to TP2 or from TP3 to TP5 including the test fixture is provided in 802.3ck 162.9.3.2.
TP2	Unless specified otherwise, all transmitter measurements defined in 802.3ck 162.9.3 are made at TP2 utilizing the test fixture specified in Annex 162B.
TP3	Unless specified otherwise, all receiver measurements and tests defined in 802.3ck 162.9.4 are made at TP3 utilizing the test fixture specified in Annex 162B.

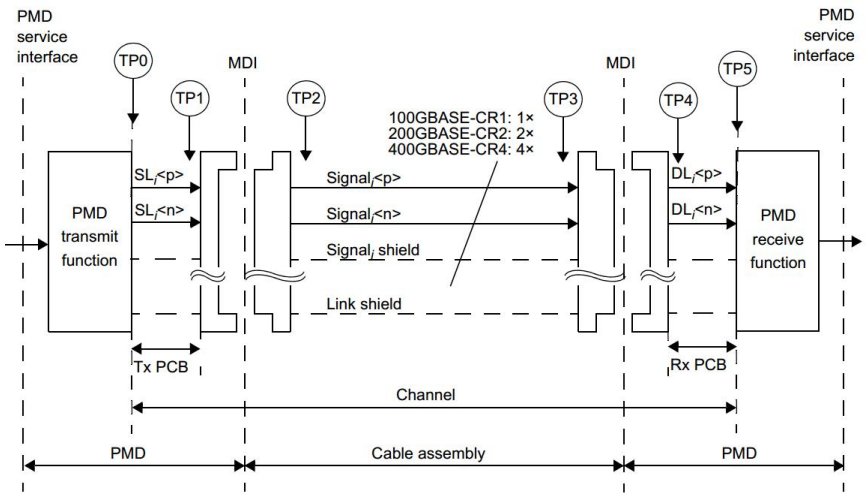

Figure 1 IEEE 802.3ck 100GBASE-CR1, 200GBASE-CR2 or 400GBASE-CR4 link

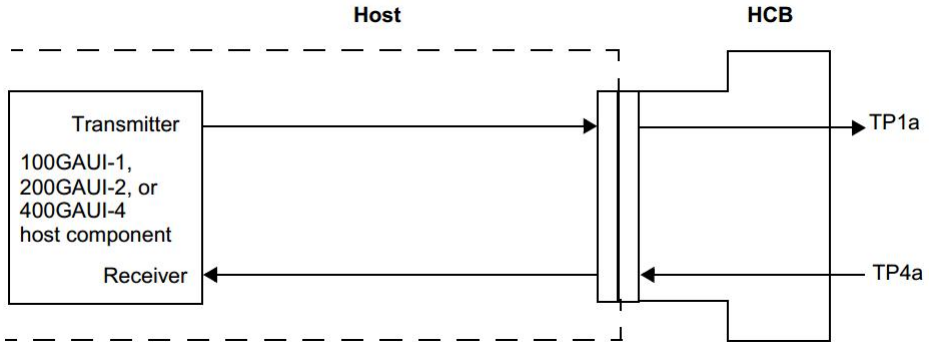

Figure 2 IEEE 802.3ck 400GAUI-4 compliance points TP1a, TP4a

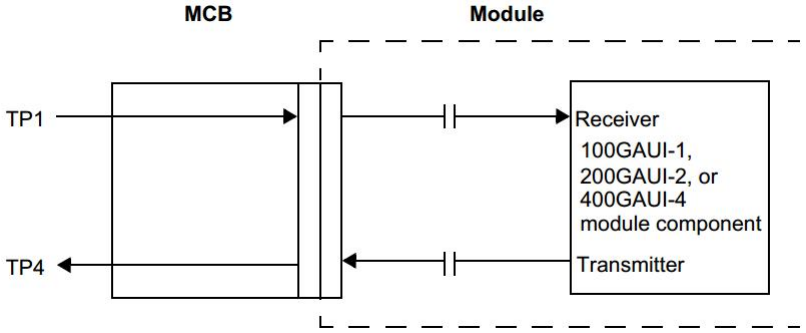

Figure 3 IEEE 802.3ck 400GAUI-4 compliance points TP1, TP4

High Speed Electrical Input Characteristics

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted.

Table4-High Speed Electrical Input Characteristics

Parameter	Test Point	Min.	Typical	Max.	Unit	Conditions
Signaling Rate, Per Lane (PAM4 encoded)	TP1		53.125		GBd	+/- 100 ppm
Differential peak-peak Input Voltage Tolerance	TP1a	750			mV	
AC common-mode RMS voltage tolerance	TP1a	25			mV	

Differential-mode to common-mode return loss	TP1	Equation (120G–2)			dB	802.3ck
Effective return loss, ERL	TP1	8.5			dB	
Differential termination mismatch	TP1a			10	%	
Module stressed input tolerance	TP1a		See 120G.3.4.3			802.3ck
Single-ended voltage tolerance range	TP1a	-0.4		3.3	V	
DC common-mode voltage tolerance range	TP1	-350		2850	mV	
Module stressed input tolerance test: Pattern generator transition time			9		ps	
Applied peak-peak sinusoidal jitter			Table 162-16			802.3ck
Eye height			10		mV	
Vertical eye closure, VEC		12		12.5	dB	
Crosstalk differential peak-to-peak voltage			845		mV	
Crosstalk transition time			8.5		ps	

High Speed Electrical Output Characteristics

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted.

Table5-High Speed Electrical Output Characteristics

Parameter	Test Point	Min.	Typical	Max.	Unit	Note

Signaling rate, per lane (range)	TP4		53.125± 100 ppm		GBd	
AC common-mode output voltage	TP4			25	mV	
Differential peak-to-peak input voltage Short mode Long mode	TP4			600 845	mV	
Eye height	TP4	15			mV	
Vertical eye closure	TP4			12	dB	
Effective return loss	TP4	8.5			dB	
Common-mode to differential-mode return loss	TP4	Equation (120G–1)			dB	
Differential termination mismatch	TP4			10	%	
Transition time	TP4	8.5			ps	
DC common-mode voltage tolerance	TP4	-0.35		2.85	V	

High Speed Optical Transmitter Characteristics

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

Table6-Optical Characteristics @TP2 Test Point

Parameter	Test Point	Min.	Typical	Max.	Unit	Note
Signaling speed per lane			53.125 ± 100ppm		GBd	
Modulation format			PAM4			
Center wavelength	λc	1304.5	1311	1317.5	nm	
Side-mode suppression ratio	SMSR	30			dB	

Extinction ratio	ER	3.5			dB	
Average launch power		-2.9		4	dBm	
OMA per lane		-0.8		4.2	dBm	
Launch Power in OMA-TDECQ, each lane		-2.2			dBm	
TDECQ (PAM4)				3.4	dB	
$RIN_{21.4}$ OMA				-136	dB/Hz	
Average launch power of OFF transmitter				-15	dBm	
Optical return loss tolerance				21.4	dB	
Transmitter Reflectance				-26	dB	

High Speed Optical Receiver Characteristics

Unless otherwise stated, the following characteristics are defined under recommended operating conditions

Table7-Optical Characteristics @TP3 Test Point

Parameter	Test Point	Min.	Typical	Max.	Unit	Note
Signaling speed per lane			53.125 ± 100ppm		GBd	
Modulation format			PAM4			
Center wavelength	λc0	1304.5	1311	1317.5	nm	
Damage threshold each lane		5			dBm	1
Average receive power each lane	Rx_{AVG}	-5.9		4	dBm	2
Receive Power (OMA_{outer}) each lane	Rx_{OMA}			4.2	dBm	
Unstressed Receiver Sensitivity (OMA) Per Lane				-4.4	dBm	1

Stressed receiver sensitivity (OMA_{outer}), each lane				-1.9	dBm	
Conditions of stressed receiver sensitivity test				3.4	dB	2
OMA_{outer} of each aggressor lane				4.2	dBm	
LOS Assert (Avg.)	LOSA	-15			dBm	
LOS De-Assert (Avg.)	LOSD			-10	dBm	
Receiver reflectance				-26	dB	

Notes:

[1] Measured with conformance test signal at TP3 for the BER specified in IEEE Std 802.3bs clause 124.1.1..
[2] These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Regulatory Compliance Issues

Various standard and regulations apply to the 800G modules. These include eye-safety,Component Recognition, RoHS, ESD, EMC and Immunity. Please note the transmitter module is a Class 1 laser product. See Regulatory Compliance Table for details.

Table8-Regulatory Compliance Table

Feature	Test Method	Performance
Laser Eye Safety and Equipment Type Testing	(IEC) EN 62368-1:2014+A11 (IEC) EN 60825-1:2014 (IEC) EN 60825-2:2004+A1+A2	CDRH Accession Number:2132182-000 TUV File: R 50457725 0001 CB File: JPTUV-100513
Component Recognition	Underwriters Laboratories (UL) and Canadian Standards Association (CSA) Joint Component Recognition for Information Technology Equipment including Electrical	UL File: E317337

	Business Equipment	
RoHS Compliance	RoHS Directive 2011/65/EU&(EU)2015/863	Less than 100 ppm of cadmium. Less than 1000 ppm lead, mercury, hexavalent chromium, poly brominated biphenyls (PPB) , poly brominated biphenyl ethers (PBDE), dibutyl phthalate, butyl benzyl phthalate, bis (2-ethylhexyl) phthalate and diisobutyl phthalates.
Electrostatic Discharge (ESD) to the Electrical Contacts	JEDEC Human Body Model (HBM)	High speed contacts shall withstand 1000V. All other contacts shall withstand 2000 V.
Electrostatic Discharge (ESD) to the Optical Connector Receptacle	IEC 61000-4-2:2008	When installed in a properly grounded housing and chassis the units are subjected to 15Kv air discharge during operation and 8Kv direct discharge to the case.
Electromagnetic Interference (EMI)	FCC Part 15 Class B; CISPR 32 (EN55032) 2015;	System margins are dependent on customer board and chassis design.
Immunity	IEC 61000-4-3:2010; EN55035:2017	Typically shows no measurable effect from a 10V/m field swept from 8MHz to 6 GHz applied to the module without a chassis enclosure.

Electrostatic Discharge (ESD)

The 800G module is complies with the ESD requirements described in the Regulatory Compliance Table. However, in the normal processing and operation of optical transceiver, the following two types of situations need special attention.

Case I: Before inserting the transceiver into the rack meeting the requirements of OSFP compliant cage, ESD preventive measures must be taken to protect the equipment. For example, the grounding wrist

strap, workbench and floor should be used wherever the transceiver is handled.

Case II: After the transceiver is installed, the electrostatic discharge outside the chassis of the host equipment shall be within the scope of system level ESD requirements. If the optical interface of the transceiver is exposed outside the host equipment cabinet, the transceiver may be subject to equipment system level ESD requirements.

Electromagnetic Interference (EMI)

Communication equipment with optical transceivers is usually regulated by FCC in the United States and CENELEC EN55032 (CISPR 32) in Europe. The compliance of 800G module with these standards is detailed in the regulatory compliance table. The metal shell and shielding design of 800G module will help equipment designers minimize the equipment level EMI challenges they face.

Flammability

The 800G module optical transceiver meets UL certification requirements, its constituent materials have heat and corrosion resistance, and the plastic parts meet UL94V-0 requirements.

OSFP Module Pad Layout

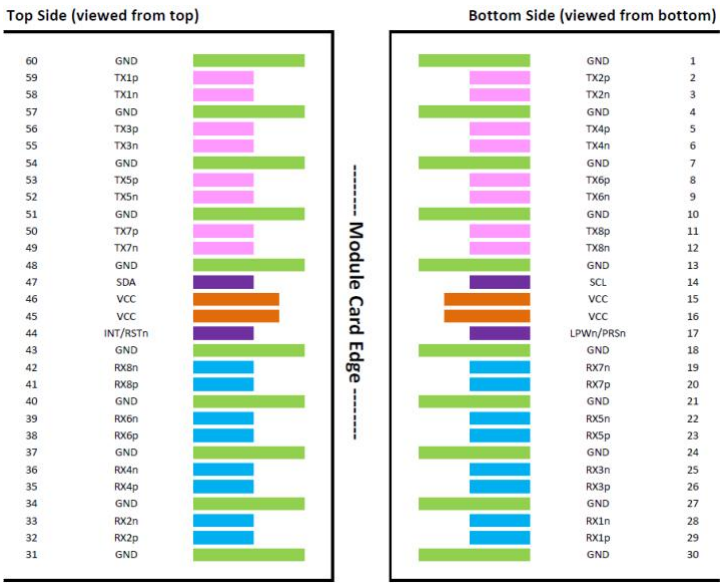

Figure 4 MSA Compliant Connector

Pin Arrangement and Definition

Table9-Pin Arrangement and Definition

Pin	Symbol	Description	Logic	Notes
1	GND	Ground		1
2	Tx2p	Transmitter Data Non-Inverted	CML-I	
3	Tx2n	Transmitter Data Inverted	CML-I	
4	GND	Ground		1
5	Tx4p	Transmitter Data Non-Inverted	CML-I	
6	Tx4n	Transmitter Data Inverted	CML-I	
7	GND	Ground		1
8	TX6p	Transmitter Data Non-Inverted	CML-I	
9	Tx6n	Transmitter Data Inverted	CML-I	
10	GND	Ground		1
11	Tx8p	Transmitter Data Non-Inverted	CML-I	
12	Tx8n	Transmitter Data Inverted	CML-I	
13	GND	Ground		1
14	SCL	2-wire serial interface clock	LVCMOS-I/O	2
15	VCC	+3.3V Power		
16	VCC	+3.3V Power		
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	
18	GND	Ground		1
19	Rx7n	Receiver Data Inverted	CML-O	
20	Rx7p	Receiver Data Non-Inverted	CML-O	
21	GND	Ground		1
22	Rx5n	Receiver Data Inverted	CML-O	
23	Rx5p	Receiver Data Non-Inverted	CML-O	
24	GND	Ground		1
25	Rx3n	Receiver Data Inverted	CML-O	
26	Rx3p	Receiver Data Non-Inverted	CML-O	
27	GND	Ground		1
28	Rx1n	Receiver Data Inverted	CML-O	
29	Rx1p	Receiver Data Non-Inverted	CML-O	
30	GND	Ground		1
31	GND	Ground		1

32	Rx2p	Receiver Data Non-Inverted	CML-O	
33	Rx2n	Receiver Data Inverted	CML-O	
34	GND	Ground		1
35	Rx4p	Receiver Data Non-Inverted	CML-O	
36	Rx4n	Receiver Data Inverted	CML-O	
37	GND	Ground		1
38	Rx6p	Receiver Data Non-Inverted	CML-O	
39	Rx6n	Receiver Data Inverted	CML-O	
40	GND	Ground		1
41	Rx8p	Receiver Data Non-Inverted	CML-O	
42	Rx8n	Receiver Data Inverted	CML-O	
43	GND	Ground		1
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	
45	VCC	+3.3V Power		
46	VCC	+3.3V Power		
47	SCL	2-wire Serial interface data	LVCMOS-I/O	2
48	GND	Ground		1
49	Tx7n	Transmitter Data Inverted	CML-I	
50	Tx7p	Transmitter Data Non-Inverted	CML-I	
51	GND	Ground		1
52	Tx5n	Transmitter Data Inverted	CML-I	
53	Tx5p	Transmitter Data Non-Inverted	CML-I	
54	GND	Ground		1
55	Tx3n	Transmitter Data Inverted	CML-I	
56	Tx3p	Transmitter Data Non-Inverted	CML-I	
57	GND	Ground		1
58	Tx1n	Transmitter Data Inverted	CML-I	
59	Tx1p	Transmitter Data Non-Inverted	CML-I	
60	GND	Ground		1

Notes:

[1] OSFP uses common ground (GND) for all signals and supply (power). All are common within the OSFP module and all module voltages are referenced to this potential unless otherwise noted.
[2] Open-Drain with pull up resistor on Host.

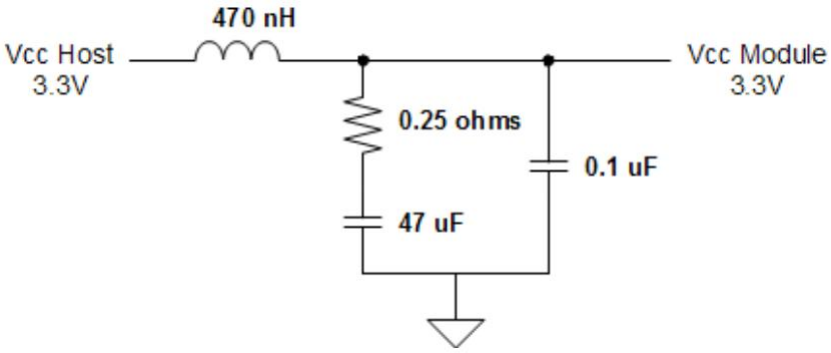

Figure 5 Recommended Host Board Power Supply Filter

For safety and protection of the host system, the power to each OSFP module may be protected by an electronic circuit breaker on the host board which is enabled with the H_PRSn signal such that power is only enabled when the module is fully engaged into the OSFP connector.

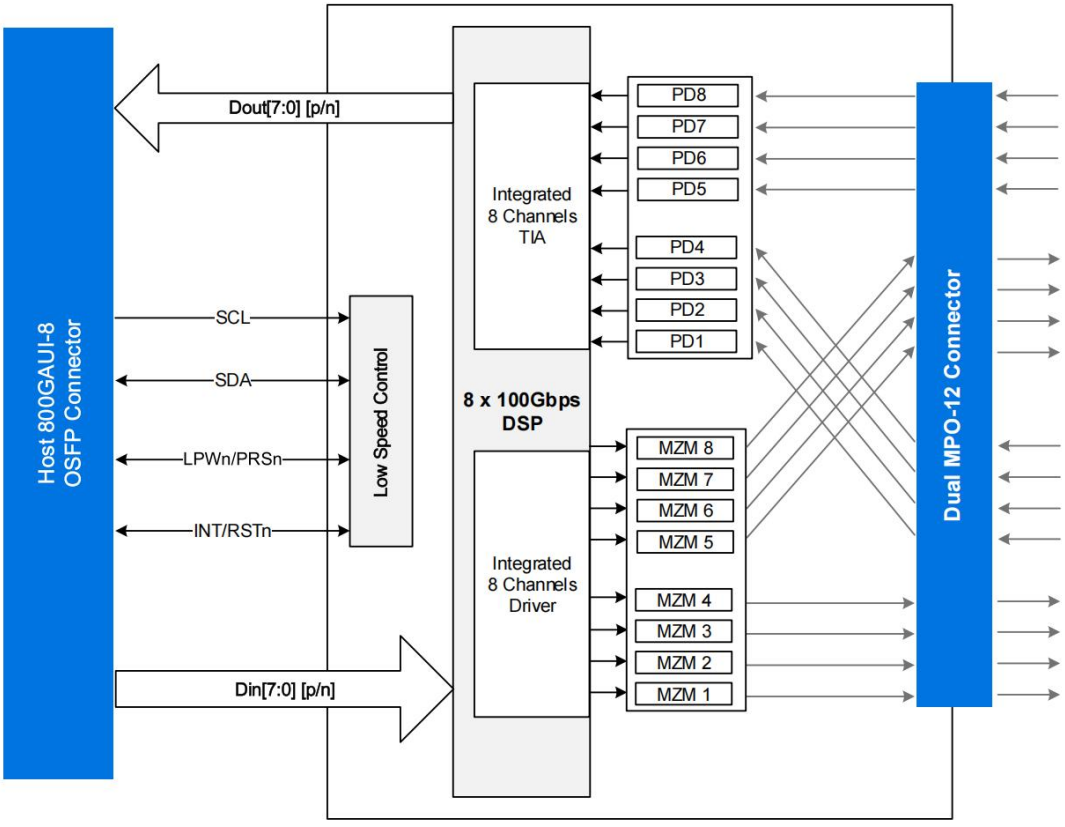

Figure 6 Transceiver Block Diagram

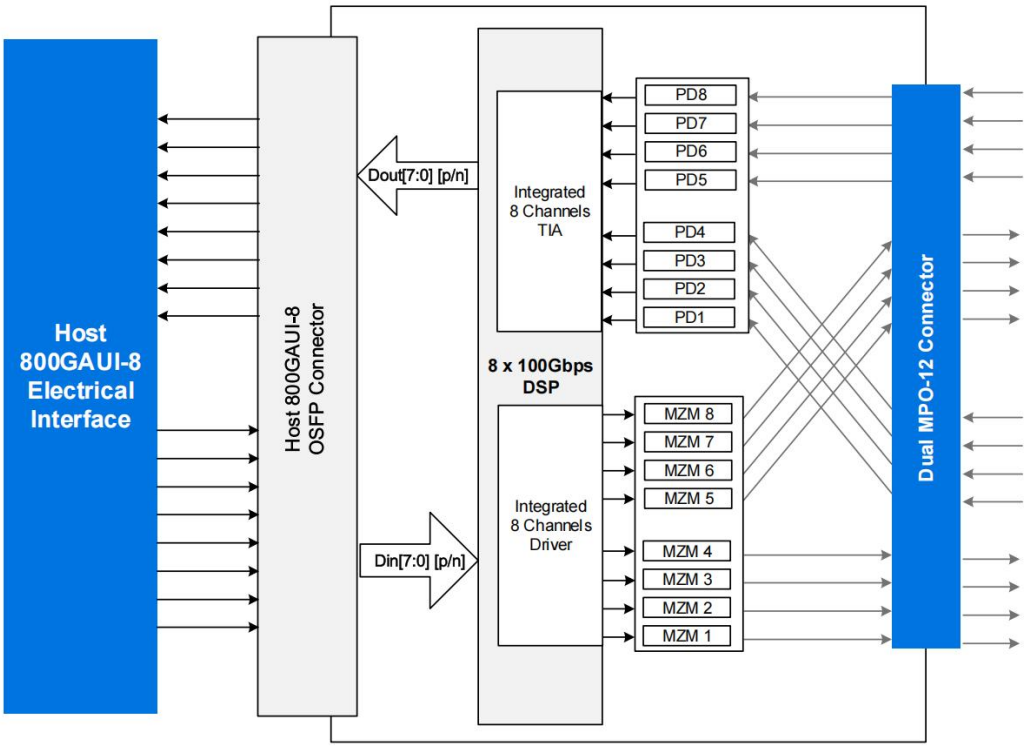

Figure 7 Application Reference Diagram

Transmitter

As shown in Figure 6, the transmitter path of the transceiver contains an 8x100Gbps 800GAUI-8 electrical input with Equalization (EQ) block, integrated electrical multiplexer, integrated driver, control and bias for the eight MZ modulators and single mode laser source. The integrated electrical multiplexer converts 8 channels of 100Gbps (PAM4) electrical input data to 8 channels of 100Gbps (PAM4) parallel optical signals.

Receiver

As shown in Figure 6, the receiver path of the transceiver contains eight PIN photodiodes, integrated TIA on the DSP, integrated electrical de-multiplexer and 8x100G 800GAUI-8 compliant electrical output blocks. The integrated de-multiplexer converts 8 channels of 100Gbps (PAM4) parallel optical signals to 8 channels of 100Gbps (PAM4) electrical output data.

High Speed Electrical Signal Interface

The interface between OSFP module and ASIC/SerDes is shown in Figure 7. The high-speed signal lines are internally AC-coupled and the electrical inputs are internally terminated to 100 Ohms differential. All transmitter and receiver electrical channels are compliant to module 800GAUI-8 specifications per IEEE 802.3ck.

Control Signal Interface

The control signal interface is compliant with OSFP MSA. The following pin is provided to control module or display the module status: LPWn/PRSn, INT/RSTn. In addition, there is an industry standard two wire serial interface scaled for 3.3V LVTTL. The definition of control signal interface and the registers of the serial interface memory are defined in the Control Interface & Memory Map section.

Handling and Cleaning

Exposure to current surges and over voltage events can cause immediate damage to the transceiver module. Observe the precautions for normal operation of electrostatic discharge sensitive equipment. Attention shall also be paid to limiting transceiver module exposure to conditions beyond those specified in the absolute maximum ratings.

Optical connectors include female connectors. These elements will be exposed as long as the cable or port plug is not inserted. At this time, always pay attention to protection.

Each module is equipped with a port guard plug to protect the optical port. The protective plug shall always be in place whenever the optical fiber is not inserted. Before inserting the optical fiber, it is recommended to clean the end of the optical fiber connector to avoid contamination of the module optical port due to dirty connector. If contamination occurs, use standard MPO port cleaning methods.

Package Outline

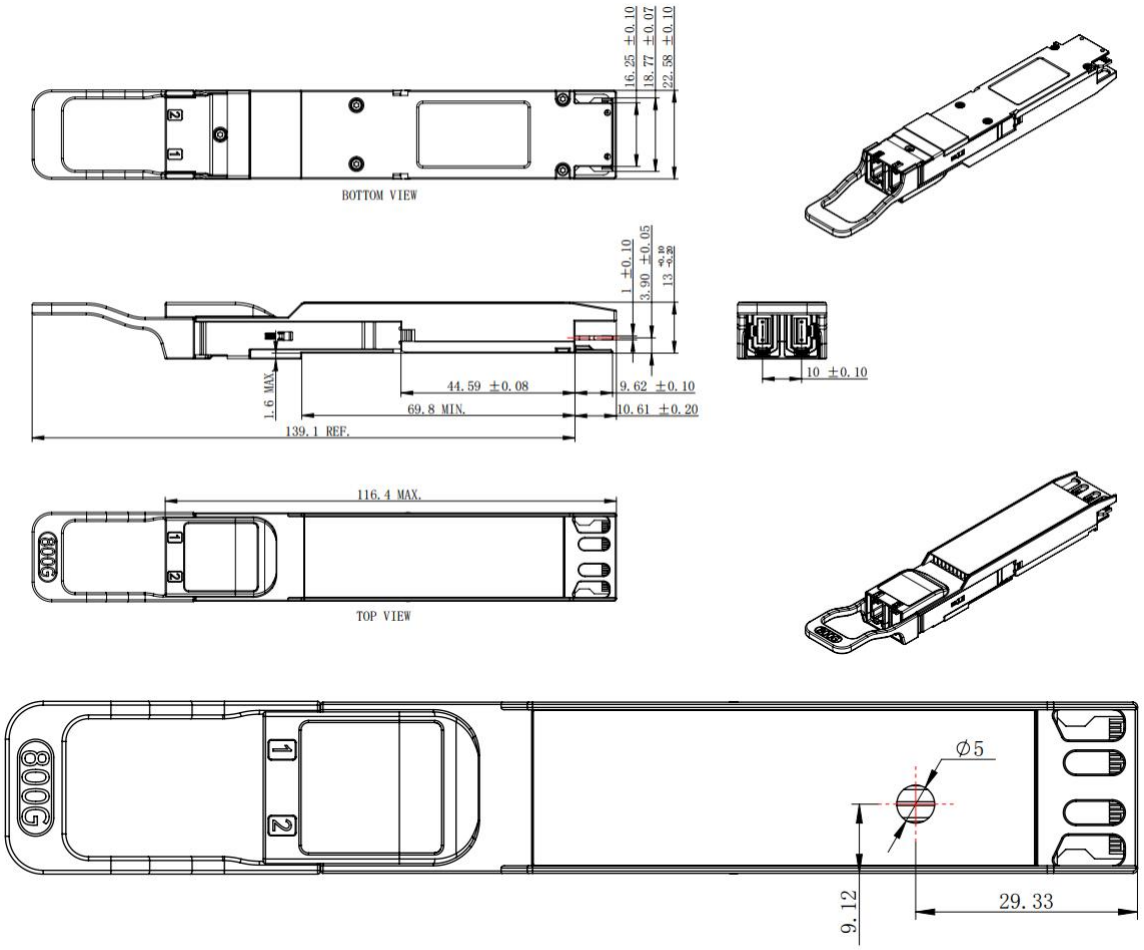

Figure 8 Closed Top Package Outline

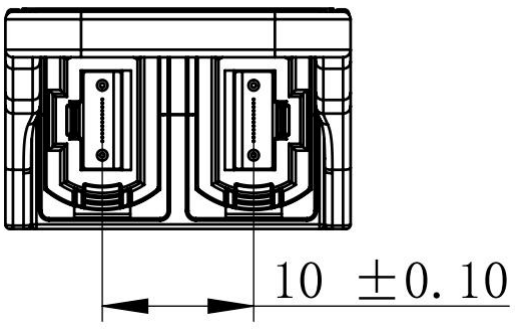

Figure 9 Module Optical Interface (looking into the optical port)

Memory Map

The control interface and memory map of the OSFP module is compliant with the CMIS. The OSFP module support I²C interface protocol defined by the CMIS. Access clock frequency is support a minimum of 100 kHz with no clock stretching.

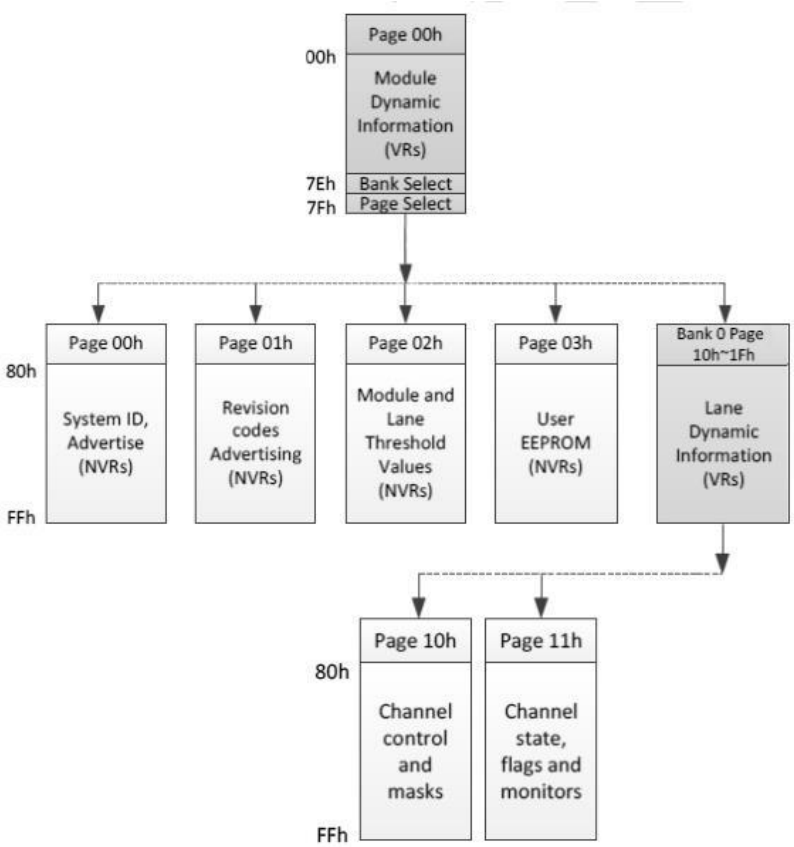

Figure 10 Simplified OSFP CMIS Module Memory Map Architecture

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