1.6T Twin-port XDR OSFP 2xFR4 2km Optical Transceiver

Features

- Supports 1.6Tbps
- Single 3.3V Power Supply
- Up to 2km over SMF with KP4 FEC supported at the Host side
- 8x226.875Gbps (PAM4) electrical interface
- Finned-top OSFP for air-cooled switches
- SMF Dual Duplex LC connector
- Power dissipation < 26W
- Case temperature range: 15°C to 70°C (commercial)
- Safety Certification: TUV/UL/FDA
- RoHS Compliant

Applications

Used in 1.6T OSFP switches

Description

OSFP-1.6T-2xFR4H transceiver module is designed for use in 1.6Tbps links over 2km single mode fiber. The module has 8 independent electrical input/output channels operating up to 226.875Gbps per channel. T his transceiver is operating on a set of wavelength on the ITU G.694.2 CWDM grid wavelength. The transmitter path of the module incorporates an 8:8 PAM4 re-timer ASIC integrated with an 8-channels high swing modulator driver, 8-channels PIC with CWDM MUX integrated and 4 CWDM CW lasers. The receiver path contains 8 photodiodes and two 4-channel TIA, along with the PAM4 re-timer. The electrical interface of the module is compliant with the 1.6TAUI-8 interface as defined by IEEE 802.3dj, and compliant with OSFP MSA.

Absolute Maximum Specifications

Absolute maximum ratings are those beyond which damage to the device may occur.

Prolonged operation between the operational specifications and absolute maximum ratings is not intended and may cause permanent device degradation.

Table1-Absolute Maximum Specifications

Parameter	Min.	Typical	Max.	Unit	Note
Storage Temperature	-40		+85	ºC	
Supply voltage	-0.5	3.3	3.6	V	
Relative Humidity (non- condensing)	5		85	%	
Data input voltage – single ended	-0.3		Vcc+0.5	V	
Data input voltage – differential			0.8	V	1
Operating Case Temperature	0		70	ºC	

Notes:

[1] This is the maximum voltage that can be applied across the differential inputs without damaging the input circuitry. The damage threshold of the module input shall be at least 1600mV peak to peak differential.

Recommended Operating Conditions

For operations beyond the recommended operating conditions, optical and electrical characteristics are not defined, reliability is not implied, and such operations for a long time may damage the module.

Table2-Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max.	Units	Note
Operating Case Temperature	Top	0		70	℃	
Power Supply Voltage	Vcc	3.135		3.465	V	
Total Power Consumption	Pc			26	W	
Electrical signal rate per channel (PAM encoded)			106.25			1
Optical signal rate per channel (PAM encoded)			113.4375			2
Power supply noise				66	mVpp	3
Receiver differential data output load		100			Ohm	
Fiber length (9μm SMF)				2	km	4

Notes:

[1] 1.6TAUI-8 operation with Host generated FEC. The transmitter must receive pre-coded FEC signals from the host ASIC.
[2] 1.6T 2xFR4 operation with Host generated FEC. The transmitter must receive pre-coded FEC signals from the host ASIC.
[3] Power Supply Noise is defined as the peak-to-peak noise amplitude over the frequency range at the host supply side of the recommended power supply filter with the module and recommended filter in place. Voltage levels including peak-to-peak noise are limited to the recommended operating range of the associated power supply.
[4] 9μm SMF. The maximum link distance is based on an allocation of 1dB of attenuation and 3 dB total connection and splice loss. The loss of a single connection shall not exceed 0.5dB.

General Electrical Characteristics

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

Table3-General Electrical Characteristics

Parameter	Min.	Typical	Max.	Unit	Note
Transceiver power consumption			26	W	
Transceiver power supply current, total			8300	mA	
AC coupling capacitors (internal)		0.1		uF	

Reference Points

For purposes of system conformance, the PMD sublayer is standardized at the points described in this subclause. The optical transmit signal is defined at the output end of a single-mode fiber patch cord (TP2), between 2 m and 5 m in length. Unless specified otherwise, all transmitter measurements and tests defined in 180.9 are made at TP2. The optical receive signal is defined at the output of the fiber optic cabling (TP3) at the MDI (see 180.8.3). Unless specified otherwise, all receiver measurements and tests defined in 180.9 are made at TP3.

TP1<0:3> and TP4<0:3> are optional reference points that may be useful to implementors for testing components (these test points will not typically be accessible in an implemented system).

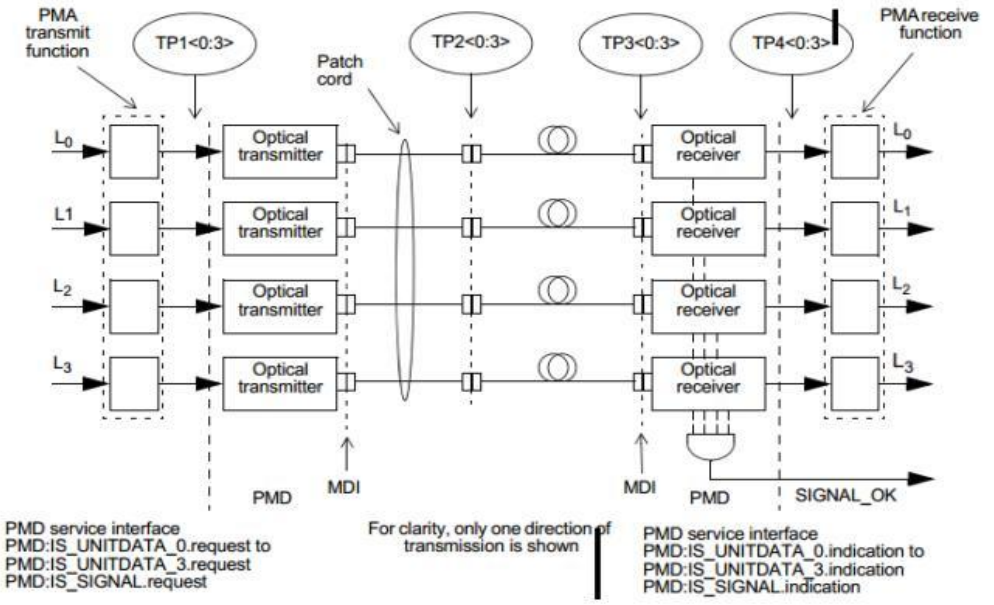

Figure 1 IEEE 802.3dj 800GBASE-DR4 transmit/receive paths

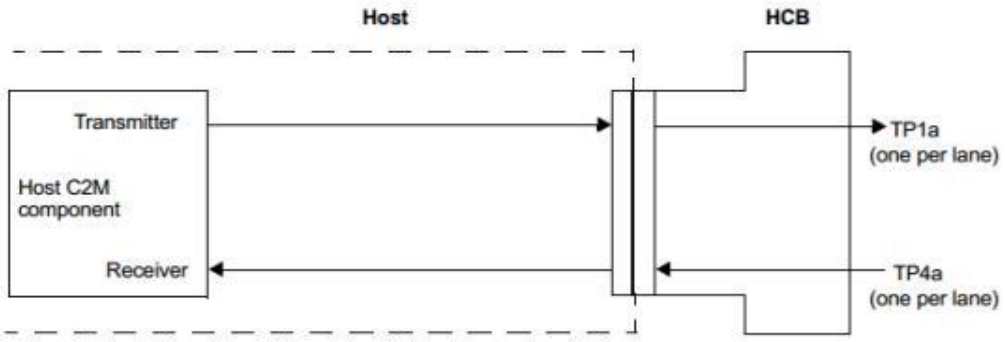

Figure 2 IEEE 802.3dj host compliance points TP1a, TP4a

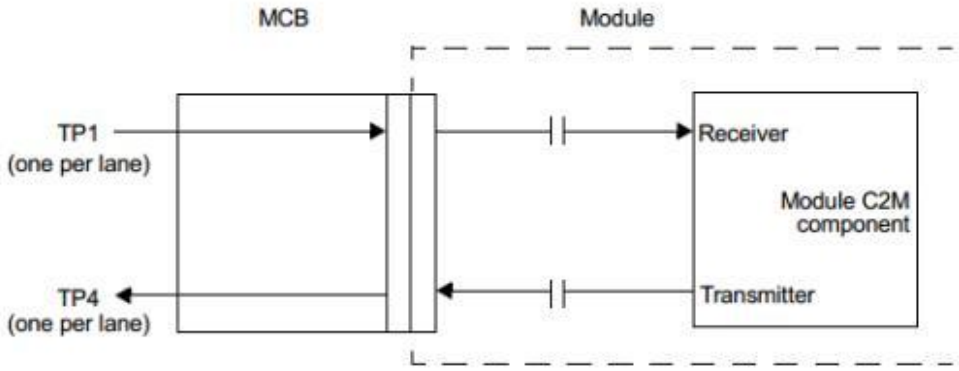

Figure 3 IEEE 802.3dj module compliance points TP1, TP4

High Speed Electrical Input Characteristics

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted.

Table4-High Speed Electrical Input Characteristics

Parameter	Test Point	Min.	Typical	Max.	Unit	Note
Signaling rate, per lane (PAM4 encoded)	TP1a		106.25±50 ppm		GBd	1
Differential peak-to-peak voltage Output enabled Output disabled	TP1a			1200 30	mV	
DC common-mode voltage (max)	TP1a			1900	mV	
AC common-mode peak-to-peak voltage Low-frequency, VCM_{LF} Full-band, VCM_{FB}	TP1a			30 85	mV	
Effective return loss, ERL	TP1a	TBD			dB	
Common-mode to common-mode return loss, RLcc	TP1a	Equation (179-9)			dB	
Common-mode to differential-mode return loss, RLdc	TP1a	Equation (179-10)			dB	
Transmitter steady-state voltage, v_f	TP1a	0.387		0.6	V	
Linear fit pulse peak ratio, R_{peak}	TP1a	TBD				
Level separation mismatch ratio, R_{LM}	TP1a					
Signal-to-noise-and-distortion ratio, SNDR(min)	TP1a	33.5			dB	

Signal-to-residual-inter symbol-interference ratio, SNR_{ISI}	TP1a	26			dB	
Output jitter (max) J_{RMS03} EOJ_{03} $J4u_{03}$	TP1a			0.023 0.025 0.135	UI	

Notes:

[1] For 200GAUI-1 or 400GAUI-2 C2M with a PMA in the same package as the PCS sublayer or for any 800GAUI-4 or 1.6TAUI-8 C2M. In other cases, the signaling rate is derived from the signaling rate presented to the PMA input lanesby the adjacent PMA or FEC sublayers.

High Speed Electrical Output Characteristics

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted.

Table5-High Speed Electrical Output Characteristics

Parameter	Test Point	Min.	Typical	Max.	Unit	Note
Signaling rate, per lane (range)	TP4		106.25 ± 50 ppm		GBd	
Differential peak-peak voltage Output enabled Output disabled	TP4			1200 30	mV	
DC common-mode voltage	TP4			1900	mV	
AC common-mode peak-to-peak voltage Low-frequency, VCM_{LF} Full-band, VCM_{FB}	TP4			30 60	mV	

Effective return loss, ERL	TP4	TBD			dB	
Common-mode to common-mode return loss, RLcc	TP4	Equation (179-9)			dB	
Common-mode to differential-mode return loss, RLdc	TP4	Equation (179-10)			dB	
Transmitter steady-state voltage, v_f	TP4	0.4		0.6	V	
Linear fit pulse peak ratio, R_{peak}	TP4	TBD				
Level separation mismatch ratio R_{LM}	TP4	0.95				
Signal-to-noise-and-distortion ratio, SNDR	TP4	33.5			dB	
Signal-to-residual-intersymbol-interference ratio, SNR_{ISI}	TP4	28			dB	
Output jitter J_{RMS03} EOJ_{03} $J4u_{03}$	TP4			0.023 0.025 0.118	UI	

High Speed Optical Transmitter Characteristics

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

Table6-Optical Characteristics @TP2 Test Point

Parameter	Test Point	Min.	Typical	Max.	Unit	Note
Signaling speed per lane			113.4375 ± 50ppm		GBd	

Modulation format		PAM4				
Center wavelength	λc0	1264.5	1271	1277.5	nm	
	λc1	1284.5	1291	1297.5	nm	
	λc2	1304.5	1311	1317.5	nm	
	λc3	1324.5	1331	1337.5	nm	
Side-mode suppression ratio	SMSR	30			dB	
Total average launch power				10.9	dBm	
Average launch power, each lane*16	TxAVG	-2.2		4.9	dBm	1
Outer optical modulation amplitude (OMAouter), each lane	OMA_{max}			4.8	dBm	
Outer optical modulation amplitude (OMA_{outer}), each lane (min) for max (TECQ, TDECQ) < 0.9 dB for 0.9dB < max (TECQ,TDECQ) < TBD dB	OMA_{max}	0.8 -0.1 + max (TECQ,TDECQ)			dBm	
Transmitter and dispersion eye closure for PAM4 (TDECQ) , each lane	TDECQ			TBD	dB	
Transmitter eye closure for PAM4 (TECQ) , each lane	TECQ			TBD	dB	
|TDECQ-TECQ|				TBD	dB	
Transmitter power excursion				2.9	dBm	
Average launch power of OFF transmitter, each lane				-16	dBm	

Extinction ratio	ER	3.5			dB	
Transmitter transition time				8	ps	
RIN17.1 OMA				-139	dB/Hz	
Optical return loss tolerance				17.1	dB	
Transmitter reflectance				-26	dB	2

Notes:

[1] Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
[2] Transmitter reflectance is defined looking into the transmitter.

High Speed Optical Receiver Characteristics

Unless otherwise stated, the following characteristics are defined under recommended operating conditions

Table7-Optical Characteristics @TP3 Test Point

Parameter	Test Point	Min.	Typical	Max.	Unit	Note
Signaling speed per lane			113.4375 ± 50ppm		GBd	
Modulation format			PAM4			
Center wavelength	λc0	1264.5	1271	1277.5	nm	
	λc1	1284.5	1291	1297.5	nm	
	λc2	1304.5	1311	1317.5	nm	
	λc3	1324.5	1331	1337.5	nm	
Damage threshold each lane			5.9		dBm	1
Average receive power each lane	Rx_{AVG}	-6.2		4.9	dBm	2
Receive Power (OMA_{outer}) each lane	Rx_{OMA}			4.8	dBm	

Difference in receive power between any two lanes (OMA_{outer})				4.1	dB	
Receiver reflectance (max)				-26	dB	
Receiver sensitivity (OMA_{outer}), each lane for TECQ < 0.9 dB for 0.9 dB < TECQ < SECQ	SenOMA	-3.7 -4.6+TECQ			dBm	3
Stressed receiver sensitivity (OMA_{outer}), each lane				TBD	dBm	4
Conditions of stressed receiver sensitivity test:						
Stressed eye closure for PAM4 (SECQ), lane under test	SECQ		TBD		dB	
LOS Assert	LOSA	-15			dBm	
LOS De-Assert	LOSD			-10	dBm	
LOS hysteresis		0.5			dB	

Notes:

[1] The receiver shall be able to tolerate, without damage, continuous exposure to an optical signal having this average power level. The receiver does not have to operate correctly at this input power.
[2] Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
[3] Measured with conformance test signal at TP3 for the BER specified in IEEE 802.3dj.
[4] Receiver sensitivity (OMA_{outer}), each lane (max) is informative and is defined for a transmitter with a value of SECQ up to 3.4dB.

Electrical to Optical Channel Mapping

Table8-Electrical to Optical Channel Mapping

Electrical Channels	Optical Wavelength (nm)

1	1271
2	1291
3	1311
4	1331
5	1271
6	1291
7	1311
8	1331

Regulatory Compliance

Various standard and regulations apply to the 1.6T modules. These include eye-safety, Component Recognition, RoHS, ESD, EMC and Immunity. Please note the transmitter module is a Class 1 laser product. See Regulatory Compliance Table for details.

Table9-Regulatory Compliance Table

Electrical Channels	Optical Wavelength (nm)
Laser Eye Safety and Equipment Type Testing	(IEC) EN 62368-1 (IEC) EN 60825-1 (IEC) EN 60825-2
Component Recognition	Underwriters Laboratories (UL) and Canadian Standards Association (CSA) Joint Component Recognition for Information Technology Equipment including Electrical Business Equipment
RoHS Compliance	RoHS Directive 2011/65/EU& (EU)2015/863
Electrostatic Discharge (ESD) to the Electrical	JEDEC Human Body Model (HBM)

Contacts	
Electrostatic Discharge (ESD) to the Optical Connector Receptacle	IEC 61000-4-2
Electromagnetic Interference (EMI)	FCC Part 15 Class B CISPR 32 (EN55032)
Immunity	IEC 61000-4-3 EN55035

Electrostatic Discharge (ESD)

The 1.6T module is complies with the ESD requirements described in the Regulatory Compliance Table. However, in the normal processing and operation of optical transceiver, the following two types of situations need special attention.

Case I: Before inserting the transceiver into the rack meeting the requirements of OSFP MSA, ESD preventive measures must be taken to protect the equipment. For example, the grounding wrist strap, workbench and floor should be used wherever the transceiver is handled.

Case II: After the transceiver is installed, the electrostatic discharge outside the chassis of the host equipment shall be within the scope of system level ESD requirements. If the optical interface of the transceiver is exposed outside the host equipment cabinet, the transceiver may be subject to equipment system level ESD requirements.

Electromagnetic Interference (EMI)

The metal shell and shielding design of 1.6T module will help equipment designers minimize the equipment level EMI challenges they face.

Flammability

The 1.6T module meets UL certification requirements, its constituent materials have heat and corrosion resistance, and the plastic parts meet UL94V-0 requirements.

OSFP Module Pad Layout

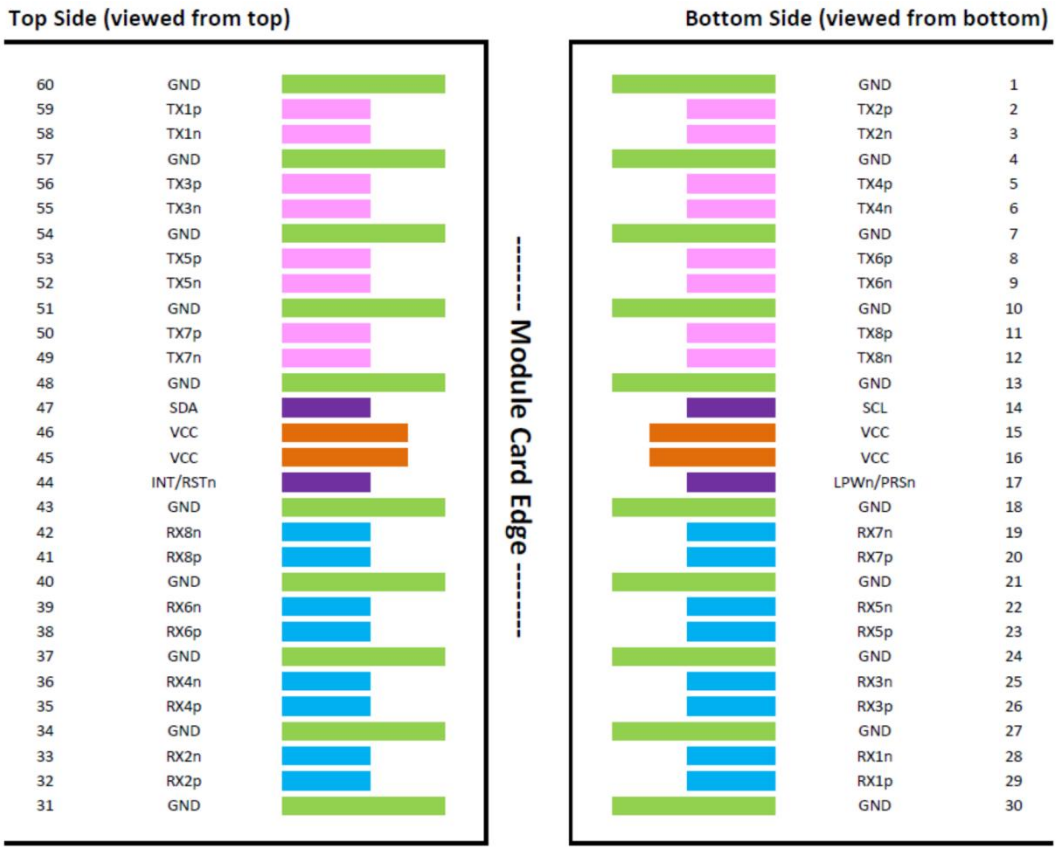

Figure 4 MSA Compliant Connector

Pin Arrangement and Definition

Table10-Pin Arrangement and Definition

Pin	Symbol	Description	Logic	Notes
1	GND	Ground		1
2	Tx2p	Transmitter Data Non-Inverted	CML-I	
3	Tx2n	Transmitter Data Inverted	CML-I	
4	GND	Ground		1

5	Tx4p	Transmitter Data Non-Inverted	CML-I	
6	Tx4n	Transmitter Data Inverted	CML-I	
7	GND	Ground		1
8	TX6p	Transmitter Data Non-Inverted	CML-I	
9	Tx6n	Transmitter Data Inverted	CML-I	
10	GND	Ground		1
11	Tx8p	Transmitter Data Non-Inverted	CML-I	
12	Tx8n	Transmitter Data Inverted	CML-I	
13	GND	Ground		1
14	SCL	2-wire serial interface clock	LVCMOS-I/O	2
15	VCC	+3.3V Power		
16	VCC	+3.3V Power		
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	
18	GND	Ground		1
19	Rx7n	Receiver Data Inverted	CML-O	
20	Rx7p	Receiver Data Non-Inverted	CML-O	
21	GND	Ground		1
22	Rx5n	Receiver Data Inverted	CML-O	
23	Rx5p	Receiver Data Non-Inverted	CML-O	
24	GND	Ground		1
25	Rx3n	Receiver Data Inverted	CML-O	
26	Rx3p	Receiver Data Non-Inverted	CML-O	
27	GND	Ground		1
28	Rx1n	Receiver Data Inverted	CML-O	
29	Rx1p	Receiver Data Non-Inverted	CML-O	
30	GND	Ground		1
31	GND	Ground		1
32	Rx2p	Receiver Data Non-Inverted	CML-O	
33	Rx2n	Receiver Data Inverted	CML-O	
34	GND	Ground		1
35	Rx4p	Receiver Data Non-Inverted	CML-O	
36	Rx4n	Receiver Data Inverted	CML-O	
37	GND	Ground		1
38	Rx6p	Receiver Data Non-Inverted	CML-O	
39	Rx6n	Receiver Data Inverted	CML-O	
40	GND	Ground		1
41	Rx8p	Receiver Data Non-Inverted	CML-O	

42	Rx8n	Receiver Data Inverted	CML-O	
43	GND	Ground		1
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	
45	VCC	+3.3V Power		
46	VCC	+3.3V Power		
47	SCL	2-wire Serial interface data	LVCMOS-I/O	2
48	GND	Ground		1
49	Tx7n	Transmitter Data Inverted	CML-I	
50	Tx7p	Transmitter Data Non-Inverted	CML-I	
51	GND	Ground		1
52	Tx5n	Transmitter Data Inverted	CML-I	
53	Tx5p	Transmitter Data Non-Inverted	CML-I	
54	GND	Ground		1
55	Tx3n	Transmitter Data Inverted	CML-I	
56	Tx3p	Transmitter Data Non-Inverted	CML-I	
57	GND	Ground		1
58	Tx1n	Transmitter Data Inverted	CML-I	
59	Tx1p	Transmitter Data Non-Inverted	CML-I	
60	GND	Ground		1

Notes:

[1] OSFP uses common ground (GND) for all signals and supply (power). All are common within the OSFP module and all module voltages are referenced to this potential unless otherwise noted.
[2] Open-Drain with pull up resistor on Host.

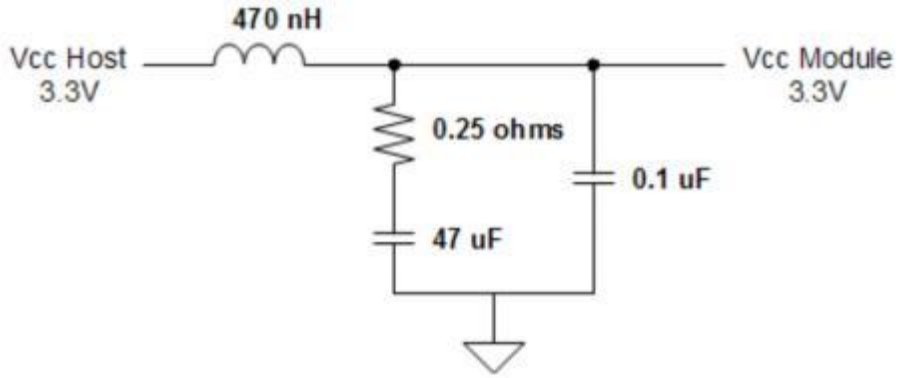

Figure 5 Recommended Host Board Power Supply Filter

For safety and protection of the host system, the power to each OSFP module may be protected by an electronic circuit breaker on the host board which is enabled with the H_PRSn signal such that power is only enabled when the module is fully engaged into the OSFP connector.

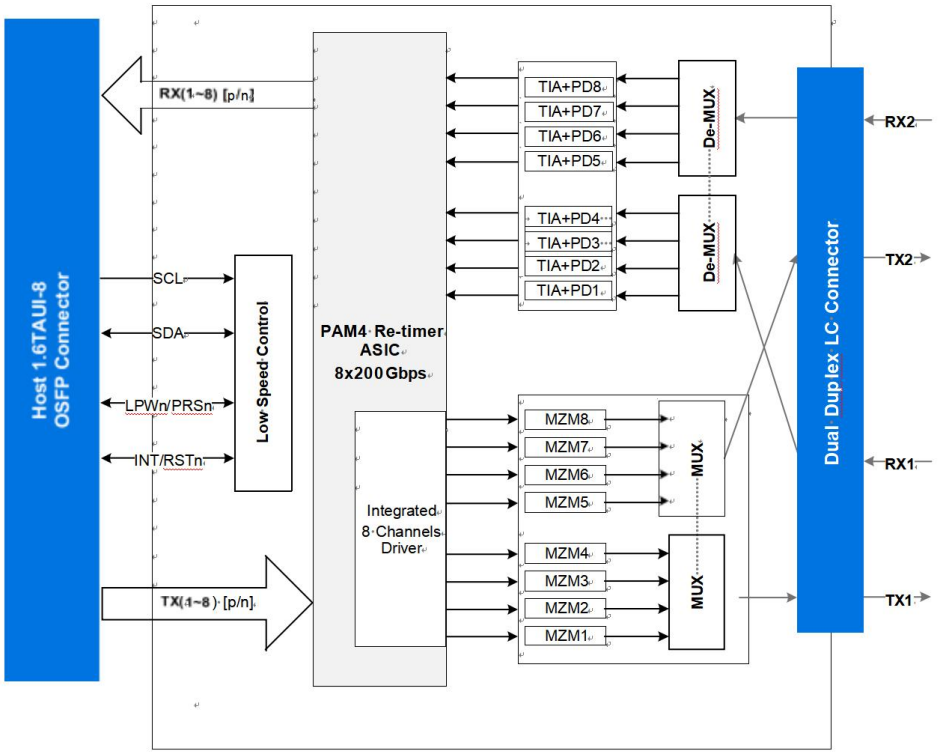

Figure 6 Transceiver Block Diagram

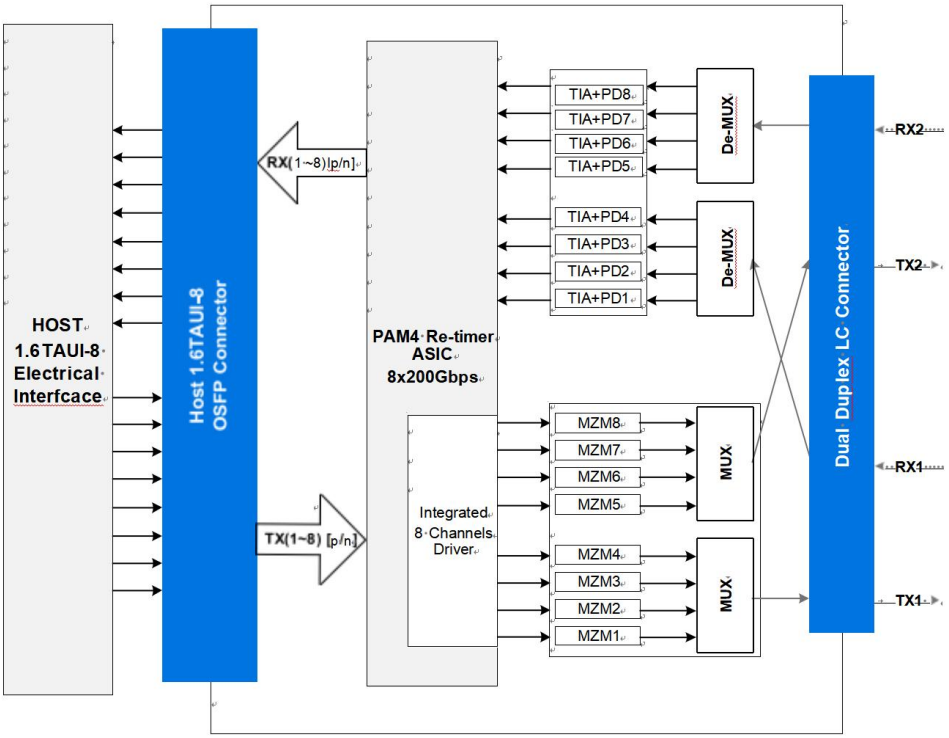

Figure 7 Application Reference Diagram

Transmitter

As shown in Figure6, the transmitter path of the transceiver contains an 8x200Gbps 1.6TAUI-8 electrical input with Equalization (EQ) block, integrated re-timer with high swing output, diagnostic monitors, single sipho PIC with 8 independent MZM modulator and 2 CWDM MUX and 4 CW CWDM lasers. The integrated electrical re-timer converts 8 channels of 100 Gbps (PAM4) electrical input data to 8 channels of 100Gbps (PAM4) high output swing optical signals. The sipho PIC modulate 8 channels of optical signal and transfer to 2 optical port. The transmitter complies with EN 60825 and CDRH Class 1 human eye safety compliance.

Receiver

As shown in Figure6, the receiver path of the transceiver contains 4 PIN photodiodes, trans-impedance amplifiers (TIA), and 8x200G 1.6TAUI-8 compliant electrical output blocks. The PIN-TIA converts 8 channels of 200Gbps (PAM4) parallel optical signals to 8 channels of 200Gbps (PAM4) electrical output data.

High Speed Electrical Signal Interface

The interface between OSFP module and ASIC/SerDes is shown in Figure 7. The high speed signal lines are internally AC-coupled and the electrical inputs are internally terminated to 100 Ohms differential. All transmitter and receiver electrical channels are compliant to module 1.6TAUI-8 specifications per IEEE 802.3dj.

Control Signal Interface

The control signal interface is compliant with OSFP MSA. The following pin is provided to control module or display the module status: LPWn/PRSn, INT/RSTn. In addition, there is an industry standard two wire serial interface scaled for 3.3V LVTTL. The definition of control signal interface and the registers of the serial interface memory are defined in the Control Interface & Memory Map section.

Handling and Cleaning

Exposure to current surges and over voltage events can cause immediate damage to the transceiver

module. Observe the precautions for normal operation of electrostatic discharge sensitive equipment. Attention shall also be paid to limiting transceiver module exposure to conditions beyond those specified in the absolute maximum ratings.

Optical connectors include female connectors. These elements will be exposed as long as the cable or port plug is not inserted. At this time, always pay attention to protection.

Each module is equipped with a port guard plug to protect the optical port. The protective plug shall always be in place whenever the optical fiber is not inserted. Before inserting the optical fiber, it is recommended to clean the end of the optical fiber connector to avoid contamination of the module optical port due to dirty connector. If contamination occurs, use standard LC port cleaning methods.

Package Outline

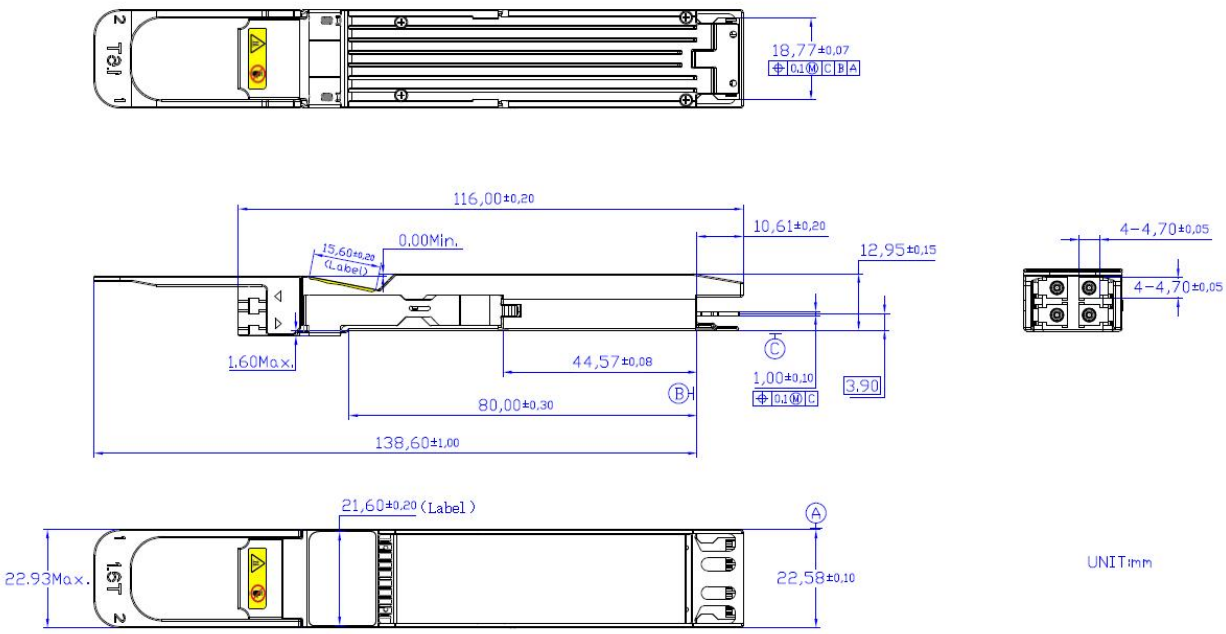

Figure 8 Package Outline

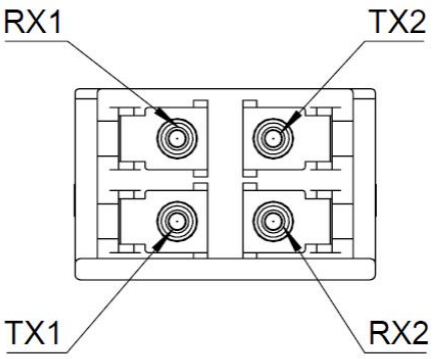

Figure 9 Module Optical Interface (looking into the optical port)

Memory Map

The control interface and memory map of the OSFP module is compliant with the CMIS. The OSFP module support I^2C interface protocol defined by the CMIS. Access clock frequency is support a minimum of 100 kHz with no clock stretching.

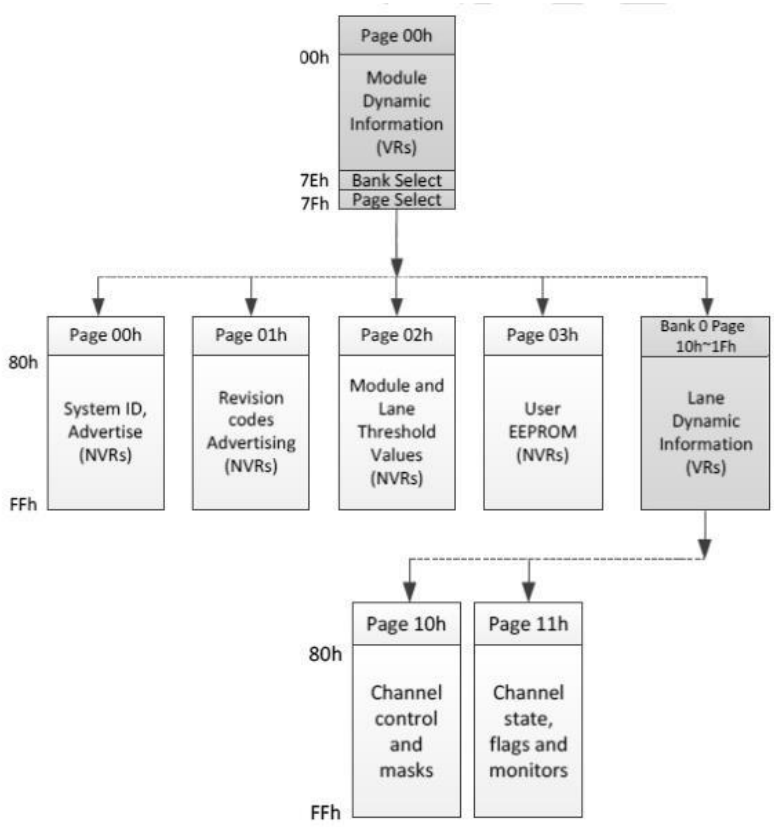

Figure 10 Simplified OSFP CMIS Module Memory Map Architecture

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