400Gb/s NDR OSFP SR4 50m Immersion Cooling Transceiver

Features

- 4x100G PAM4 retimed 400GAUI-4 electrical interface
- MPO-12 Female/Male plug tail fiber
- 4 channel VCSEL arrays and 4 channels PIN photo detector arrays
- Maximum link length of 50m
- Supports liquid cooling
- Hot Pluggable OSFP form factor
- Compliant to OSFP Module Specification Rev 5.0
- Compliant with CMIS 5.2
- Compliant with IEEE 802.3db
- Compliant to IEEE 802.3ck
- Less than 9W in temperature range of 10 to 60℃

Applications

- 400GBASE-SR4 400G InfiniBand/Ethernet (immersion cooling)
- Data center (immersion cooling)

Description

NADDOD 400G OSFP SR4 transceiver modules are high performance modules that support Immersion cooling for short-range data communication and interconnect application. They integrate four data lanes in each direction with 4x106.25GBd. The length of OSFP SR4 is up to 50 meters. They are compliant with the OSFP MSA , IEEE 802.3 db and CMIS 5.2.

Absolute Maximum Ratings and Recommended Operating Conditions

Table1-Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Storage Temperature	Ts	-40	85	℃
Case Operating Temperature	Top	10	60	℃
Relative Humidity (non-condensation)	RH	15	85	%
Supply Voltage	Vcc	-0.5	3.6	V
Receiver Damage Threshold, per Lane	PRdmg	5		dBm

Table2-Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Operating Case Temperature	Top	10	60	℃
Relative Humidity(non-condensing)	RH	15	85	%
Power Supply Voltage	Vcc	3.135	3.465	V
Total Power Consumption[1]	Pc		9	W
Supply Current			2.87	A
Bit Rate	BR		425	Gbps
Fiber Length on OM3 MMF			30	m
Fiber Length on OM4 MMF			50	m
I2C Clock Frequency		0	1000	kHz

Notes:

[1] Under condition of 3.465V operating supply voltage, and 60℃ case temperature

Electrical Specifications

Table3-Electrical Specifications

Parameter	Typical	Max.	Unit	Note
Pre FEC Bit Error Ratio			2.4E-4	
Post FEC Bit Error Ratio			1E-12	
Transmitter (each Lane)				
Differential pk-pk Input Voltage tolerance	750			mV
Differential Termination Mismatch			10	%
Eye height	10			mV
Common-mode to differential-mode return loss	IEEE802.3ck Equation (120G–1)			dB
Vertical eye closure			12	dB
Effective return loss	7.3			dB
Transition Time	10			ps
Receiver (each Lane)				
Differential data output swing	300		900	mVpp
Differential termination mismatch			10	%
Eye height	15			mV

Vertical eye closure			12	dB
Common-mode to differential-mode return loss	IEEE802.3ck Equation (120G–1)			
Effective return loss	8.5			dB
Transition time	8.5			ps

Optical Specifications

Table4-Transmitter Optical Interface

Parameter		Symbol	Min.	Typical	Max.	Unit
Data rate per lane		DR		53.125		GBd
Modulation format				PAM4		
Center Wavelength [1]		λ	840	860	868	nm
RMS spectral width		σ			0.6	nm
Average Launch power, each lane		Pavg	-1		4	dBm
Optical Power OMA, each Lane , max		POMA		3.5		dBm
OMAouter, each lane min	max (TECQ, TDECQ) <1.8 dB		max [-2.6 , max(TECQ,TECQ)– 4.4]			dBm
	1.8 < max (TECQ, TDECQ) < 4.4 dB					
Transmitter and dispersion eye closure (TDECQ), each lane		TDECQ			4.4	dB
Transmitter eye closure for PAM4 (TECQ), each lane		TECQ			4.4	dB
Extinction ratio		ER	2.5			dB
Transmitter power excursion, each lane					2.3	dBm
Optical Return Loss Tolerance		ORLT			14	dB
Optical Power for TX DISABLE					-30	dBm
Encircled fluxb[2]			≥86% at 19 um ≤30% at 4.5 um			

Notes:

[1] Defined according to the performance of the laser used.

[2] Measured into type A1a.2 or type A1a.3, or A1a.4, 50 um fiber, in accordance with IEC 61280-1-4.

Table5-Receiver Optical Interface

Parameter	Symbol	Min.	Typical	Max.	Unit
Data rate per lane	BR		53.125		Gbd
Modulation format			PAM4		
Center Wavelength	λ	842	850	948	nm
Damage threshold		5			dBm
Average receive power, each lane		–6.4		4	dBm

Receive power, each lane (OMAouter)					3.5	dBm
Receiver reflectance		Rr			–15	dB
Receiver sensitivity, each lane[1]			RS = max (-4.6 , TECQ – 6.4)			dBm
Stressed receiver sensitivity, each lane					–2	dBm
Rx LOS	Assert		-15			dBm
	De-assert				-7.5	dBm
	Hysteresis		0.5		5	dB

Notes:

[1] Receiver sensitivity is informative and is defined for a transmitter with a value of TECQ. Measured with conformance test signal at TP3 for BER = 2.4E-4 Pre-FEC.

Pin Description

OSFP Transceiver Pad Layout, host PCB OSFP Pinout, and PIN Descriptions are as follows:

Table6-Pin Description

Pin	Symbol	Description	Pin	Symbol	Description
1	GND	Ground	31	GND	Ground
2	Tx2p	Transmitter Non-Inverted Data Input	32	Rx2p	Receiver Non-Inverted Data Output
3	Tx2n	Transmitter Inverted Data Input	33	Rx2n	Receiver Inverted Data Output
4	GND	Ground	34	GND	Grounds
5	Tx4p	Transmitter Non-Inverted Data Input	35	Rx4p	Receiver Non-Inverted Data Output
6	Tx4n	Transmitter Inverted Data Input	36	Rx4n	Receiver Inverted Data Output
7	GND	Ground	37	GND	Ground
8	Tx6p	Transmitter Non-Inverted Data Input	38	Rx6p	Receiver Non-Inverted Data Output
9	Tx6n	Transmitter Inverted Data Input	39	Rx6n	Receiver Inverted Data Output
10	GND	Ground	40	GND	Ground
11	Tx8p	Transmitter Non- Inverted Data input	41	Rx8p	Receiver Non-Inverted Data Output
12	Tx8n	Transmitter Inverted Data Input	42	Rx8n	Receiver Inverted Data Output
13	GND	Ground	43	GND	Ground
14	SCL	2-wire serial interface clock	44	INT / RSTn	Module Interrupt / Module Reset
15	VCC	+3.3V Power	45	VCC	+3.3V Power
16	VCC	+3.3V Power	46	VCC	+3.3V Power
17	LPWn / PRSn	Low-Power Mode / Module Present	47	SDA	2-wire Serial interface data
18	GND	Ground	48	GND	Ground
19	Rx7n	Receiver Inverted Data Output	49	Tx7n	Transmitter Inverted Data Input

20	Rx7p	Receiver Non-Inverted Data Output	50	Tx7p	Transmitter Non-Inverted Data Input
21	GND	Ground	51	GND	Ground
22	Rx5n	Receiver Inverted Data Output	52	Tx5n	Transmitter Inverted Data Input
23	Rx5p	Receiver Non-Inverted Data Output	53	Tx5p	Transmitter Non-Inverted Data Input
24	GND	Ground	54	GND	Ground
25	Rx3n	Receiver Inverted Data Output	55	Tx3n	Transmitter Inverted Data Input
26	Rx3p	Receiver Non-Inverted Data Output	56	Tx3p	Transmitter Non-Inverted Data Input
27	GND	Ground	57	GND	Ground
28	Rx1n	Receiver Inverted Data Output	58	Tx1n	Transmitter Inverted Data Input
29	Rx1p	Receiver Non-Inverted Data Output	59	Tx1p	Transmitter Non-Inverted Data Input
30	GND	Ground	60	GND	Ground

OSFP Module Pad Layout

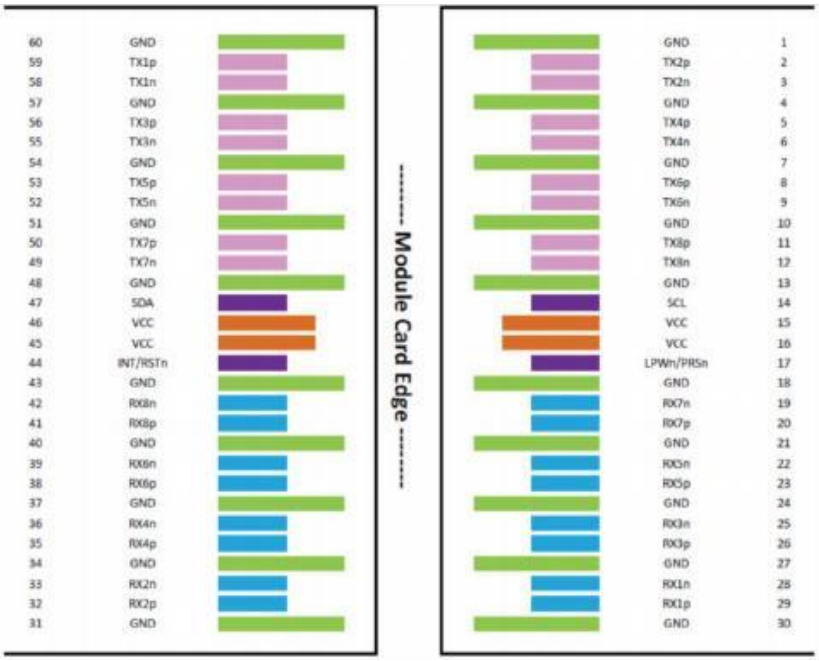

Figure 1 MSA Compliant Connector

Management Interface

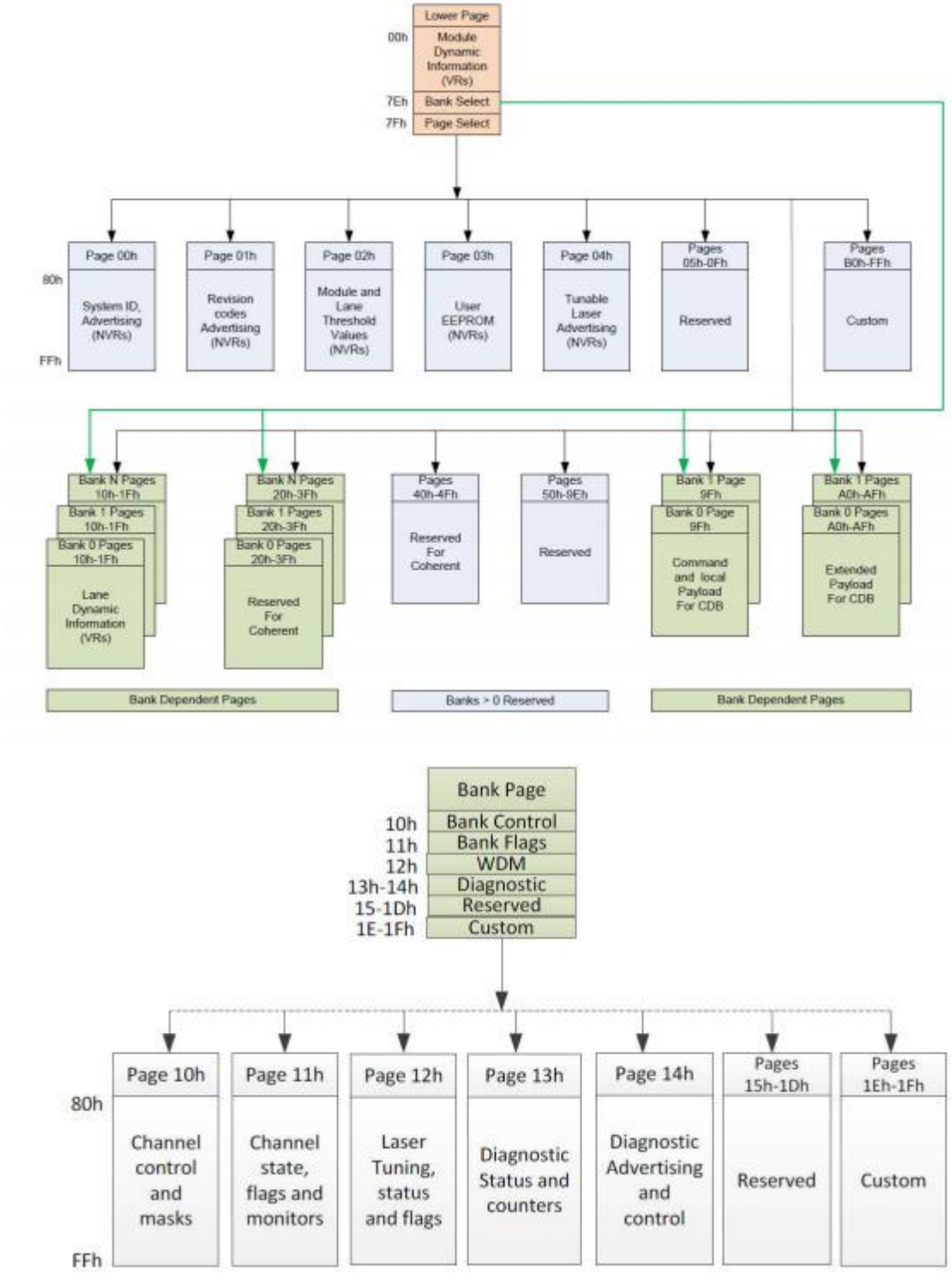

Figure2 CMIS Module Memory Map

Multiple Applications Support

It support CMIS 5.2 defined Application Advertising, Application Selection and Instantiation

Application Advertising

Table7-Application Advertising

Address (Dec)	Application		Value (Hex)	Description
	AppSel Code	Name		
85	NA	Module Type encoding	1	Optical Interfaces: MMF
86	0001b	HostInterfaceID	4B	HostInterfaceIDApp1:100GAUI-1-S C2M
87		MediaInterfaceID	D	MediaInterfaceIDApp1:100GBASE-SR
88		HostLaneCount& MediaLaneCount	11	LaneCountApp1 ： TX & RX 1 lanes
89		HostLaneAssignmentOptions	F	Permissible first host lane number: lanes 1, 2, 3, 4,
01h:176		MediaLaneAssignmentOptions	F	Permissible first media lane number: lanes 1, 2, 3, 4
90	0010b	HostInterfaceID	F	HostInterfaceIDApp2:200GAUI-4
91		MediaInterfaceID	E	MediaInterfaceIDApp2:200GBASE-SR4
92		HostLaneCount& MediaLaneCount	44	LaneCountApp2:TX & RX 4 lanes
93		HostLaneAssignmentOptions	1	Permissible first host lane number: lane 1
01h:177		MediaLaneAssignmentOptions	1	Permissible first media lane numbern: lane 1
94	0011b	HostInterfaceID	C	HostInterfaceIDApp3:100GAUI-4 C2M
95		MediaInterfaceID	0	MediaInterfaceIDApp3: SFF-8024 Undefined
96		HostLaneCount& MediaLaneCount	44	LaneCountApp3:TX & RX 4 lanes
97		HostLaneAssignmentOptions	1	Permissible first host lane number: lane 1
01h:178		MediaLaneAssignmentOptions	1	Permissible first media lane number: lane 1
98	0100b	HostInterfaceID	4F	HostInterfaceIDApp4:400G S C2M
99		MediaInterfaceID	11	MediaInterfaceIDApp4:400G-SR4
100		HostLaneCount& MediaLaneCount	44	LaneCountApp4:TX & RX 4 lanes
101		HostLaneAssignmentOptions	1	HostLaneAssignmentOptionsApp4:begin lane 1
01h:179		MediaLaneAssignmentOptions	1	Permissible first media lane number: lane 1
102	0101b	HostInterfaceID	4D	HostInterfaceIDApp5:200GAUI-2-S C2M
103		MediaInterfaceID	1B	MediaInterfaceIDApp5:200GBASE-SR2
104		HostLaneCount& MediaLaneCount	22	LaneCountApp5 ： TX & RX 2 lanes
105		HostLaneAssignmentOptions	5	Permissible first host lane number: lanes 1, 3,
01h:180		MediaLaneAssignmentOptions	5	Permissible first media lane number: lanes 1, 3

106			FF	HostInterfaceIDApp6
107			0	MediaInterfaceIDApp6
108			0	LaneCountApp6
109			0	HostLaneAssignmentOptionsApp6
110			0	HostInterfaceIDApp7
111			0	MediaInterfaceIDApp7
112			0	LaneCountApp7
113			0	HostLaneAssignmentOptionsApp7

As shown in the table above , they support 5 applications,400GBASE-SR4, 200GBASE- SR4, 100GBASE-SR4,2X200GBASE-SR2,4X100GBASE-SR1.

Application Selection and Instantiation

The host can select Applications by programming the AppSel value in Staged Set 0. AppSel=1 is the default Application populated in the Active Control Set at power-on or reset.

**Note that the channels of the module are independent and can be configured separately.(ie. up to eight 100GBASE-SR instances can be configured), however, it does not support different applications with different channels at the same time*

It support two methods of application selection and instantiation. The first method is implemented according to CMIS, and the second method is customized , which is simpler.

First mothod:

The applications switching configuration sequence is as follows: read Application Descriptor Registers and select the required Appsel. Write application configuration to DPConfigLane<i> in Stage Control Set 0,then write 1 to ApplyDPInitLane<i> to trigger Application Instantiation.

The Active Set can be read from page11h. For example, select AppDescriptor3:

Step 1: Write 0x30 in Page10h Byte145~Byte152(8 bytes)—Set AppselCode3

Step 2: Write 0xFF in Page10h Byte143—Set trigger register to run Application Instantiation.

Second mothod:

Set the value of Page10h Byte240. This is a private definition.

Table8-Private Host Electrical Interface Codes

Code Value	Bit Pattern	Host Electrical Interface	Media Interface
0	00000000b	100GAUI-1-S C2M	100GBASE-SR1
1	00000001b	200GAUI-4	200GBASE-SR4
2	00000010b	100GAUI-4	100GBASE-SR4
3	00000011b	400GAUI-4-S C2M	400GBASE-SR4
4	00000100b	200GAUI-2-S C2M	200GBASE-SR2

TX & RX Squelch

Default TX and RX auto-squelch is enabled. But TX and RX auto squelch disable, and force squelching function are not supported.

TX input equalization

Default TX adaptive equalization is enabled. But TX adaptive equalization disable, and fixed equalization adjust function are not supported.

RX output Equalization

RX output Equalization follows CMIS Table 6-7, with default 1dB, readable and writable

Table 6-7 Rx Output Equalization Codes

Code Value	Bit pattern	Post-Cursor Equalization	Pre-Cursor Equalization
0	0000b	0dB (No Equalization)	0dB (No Equalization)
1	0001b	1 dB	0.5 dB
2	0010b	2 dB	1.0 dB
3	0011b	3 dB	1.5 dB
4	0100b	4 dB	2.0 dB
5	0101b	5 dB	2.5 dB
6	0110b	6 dB	3.0 dB
7	0111b	7 dB	3.5 dB
8-10	1000b-1010b	**Reserved**	**Reserved**
11-15	1011b-1111b	Custom	Custom

RX output amplitude

RX output amplitude follows CMIS Table 6-8, Rx output amplitude is the difference peak-to- peak EYE high when Rx output equalization is set to 0dB. The default value of output amplitude is set to 2, with typical differential 600mVp-p.

Table 6-8 Rx Output Amplitude Codes

Code Value	Bit pattern	Output Amplitude
0	0000b	100-400 mV (P-P)
1	0001b	300-600 mV (P-P)
2	0010b	400-800 mV (P-P)
3	0011b	600-1200 mV (P-P)
4-14	0100b-1110b	**Reserved**
15	1111b	Custom

Loopback capabilities

Media side input loopback and Host side input loopback feature are supported, loopback control method refers to CMIS.

Table9-Rx Output Equalization code table

Byte	Bits	Field Name	Field Description

13h:128	6	Simultaneous Host And Media Side loopbacks	0b: not supported
	5	Per Lane Media Side Loopbacks	1b: supported
	4	Per Lane Host Side Loopbacks	1b: supported
	3	Host Side Input Loopback	1b: supported
	2	Host Side Output Loopback	1b: supported
	1	Media Side Input Loopback	1b: supported
	0	Media Side Output Loopback	1b: supported

Digital Diagnostic Monitor Accuracy

The following characteristics are defined over recommended operating conditions.

Table10-Digital Diagnostic Monitor Accuracy

Parameter	Accuracy	Unit
Internally measured transceiver temperature[1]	+/-3	℃
Internally measured transceiver supply voltage	+/-3	%
Measured Tx bias current	+/-10	%
Measured Tx output power[2]	+/-3	dB
Measured Rx received average optical power	+/-3	dB

Notes:

[1] Test point is the hotspot of the module.

[2]. DDM reports stability within 0.5 dB when temperature is stable. TX DDM reportes -40 dBm when TX disable.

Transceiver Block Diagram

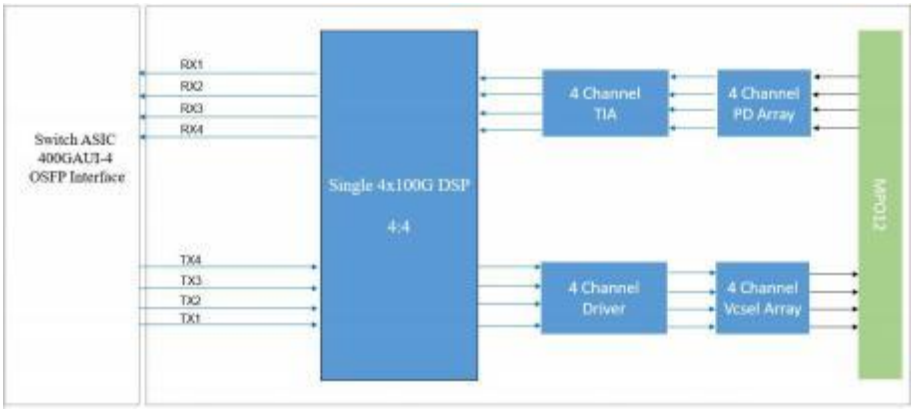

Figure 3. Transceiver Block Diagram

Mechanical Dimensions

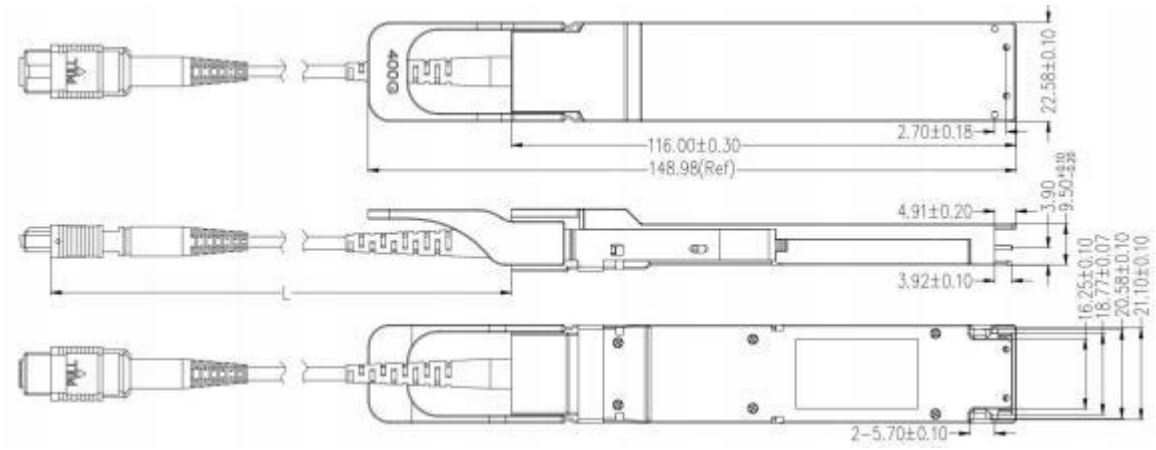

Figure4 Package dimensions (female)

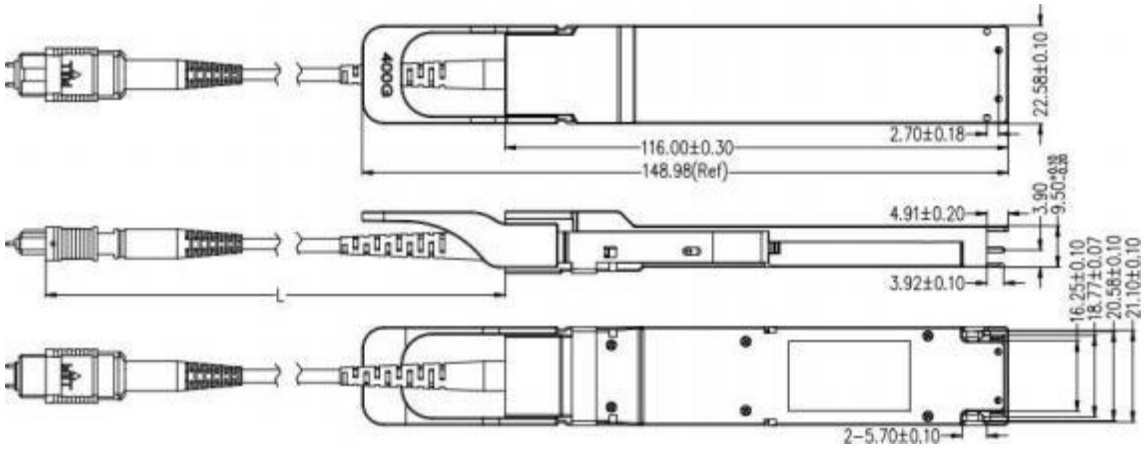

Figure5 Package dimensions (male)

Optical interface requirement:

The optical port is a tail fiber of the MPO12 female.

The optical port is a tail fiber of the MPO12 male plug.

Laser safety and Electromagnetic Compatibility

Laser safety

They are Class 1 Laser products according to FDA/CDRH、 IEC-60825-1 and IEC60825-2 standards. They must be operated under the specified operating conditions

Electromagnetic Compatibility

They are designed to meet FCC Class B limits.

Further Information:

Web www.naddod.com

Email

For order requirements: sales@naddod.com

For customer service: support@naddod.com

For technical support: tech@naddod.com

For cooperation: agency@naddod.com

For other informations: info@naddod.com

Disclaimer

1. We are committed to continuous product improvement and feature upgrades, and the contents contained in this manual are subject to change without notice.

2. Nothing herein should be construed as constituting an additional warranty.

3. NADDOD assumes no responsibility for the use or reliability of equipment or software not provided by NADDOD.